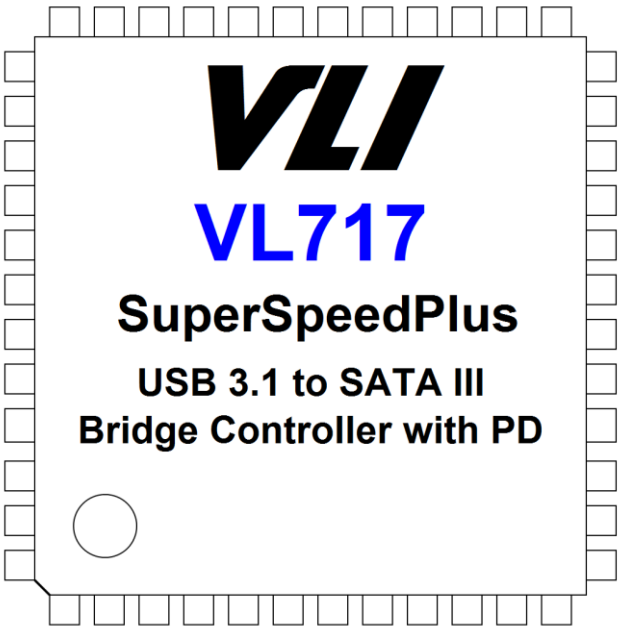
VIA Labs, Inc.

Data Sheet

VL717
USB 3.1 Gen2 to SATA 6GB/s Bridge Controller with PD Sink for USB-C

August 16th , 2018

Revision 0.90



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Revision History

Rev	Date	Note	Initial
0.90	08/16/2018	Preliminary release	HC

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Product Features

VL717
USB 3.1 Gen2 to SATA 6GB/s Bridge Controller with PD Sink for USB-C

■USB 3.1 Gen2 (10GB/s) and USB High-Speed (480Mb/s)
– Compliant to Universal Serial Bus 3.1 Specification Revision 1.0
– Compliant to Universal Serial Bus Specification Revision 2.0
– Mass Storage Class Bulk-Only Transport (BOT)
– USB Attached SCSI Protocol (UASP) for streaming
– Integrated in-house USB 3.1 Gen2 PHY and USB2.0 PHY

■Serial ATA 6GB/s, 3GB/s and 1.5GB/s
– Compliant to Serial ATA Specification Revision 3.1
– Integrated in-house SATA 6GB/s PHY
– RBC command conversion for ATA device
– MMC-2 command pass-through to ATAPI
– Support 48-bit LBA and multiple LUN

■Fast 8051 Macro cell 80C32-Compatible Microcontroller
– Standard 1T 8051 instruction set

■USB Type-C connector support
– Compliant to USB Power Delivery Specification Revision 3.0 Version 1.1 at PD sink mode
– CC1/CC2 cable orientation detection logic
– Two sets of USB signal pins to enable USB-C cable flipping feature

■Built-in Voltage Regulators
– 5.0V to 3.3V LDO
– 5.0V to 1.2V switching DC-DC

■GPIOs for Special Function Usage
– 6 GPIOs for customer special usage
– 2 dedicated BUSY/POWER LED indicators

■Misc
– Support device power down function
– Support external SPI flash for firmware upgrade

■Software
– Support Microsoft Windows 10, Windows 8, Windows 7, Vista, XP
– Support Mac OS 10.X
– Support various Linux kernels

■Physical
– QFN 48L green package (6x6x0.85 mm)

■Certification
– USB-IF USB 3.1 Gen2 Certified: TBD

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VL717 System Overview

VIA Lab's VL717 is a high performance, low power single chip USB 3.1 Gen2 to SATA 6GB/s bridge controller with PD sink mode support for USB type-C connector designed for new generation external storage devices. Its integrated in-house USB 3.1 Gen2 PHY enables VL717 to run in USB 3.1 Gen2, USB 3.1 Gen 1, High-Speed, and Full-Speed modes. Supporting USB mass storage class Bulk-Only Transport (BOT), VL717 based devices can work on Windows 10, Windows 8, Windows 7, Vista, XP, Mac OS X and various Linux kernels without additional driver. Besides Bulk-Only Transport, VL717 also support USB Attached SCSI Protocol (UASP) that allowing mass storage command queuing and out of order data transfers to further enhance read/write performance. Its integrated in-house SATA 6GB/s host controller can work with all SATA based storage devices and can connect at SATA 6GB/s, SATA 3GB/s, or SATA 1.5GB/s automatically. Built-in CC1/CC2 cable orientation detection circuits and two sets of USB signal pins, VL717 can support USB type-C receptacle natively with good signal integrity to enable USB-C cable flipping feature without any extra cost. VL717 also support Power Delivery sink mode that can check host power capability and ask host to source its maximum power.

Built-in all required linear and switching voltage regulators, highly integrated VL717 work perfectly with single power input from USB 5V bus power to save customer BOM cost. Up to eight GPIO pins are available for push button, operation LEDs, device power down control, and other special usage. The SPI interface can support external flash for firmware upgrades or additional software enhancements. VL717 is available in QFN 48L (6x6x0.85 mm) green packages to fit small form-factor design.

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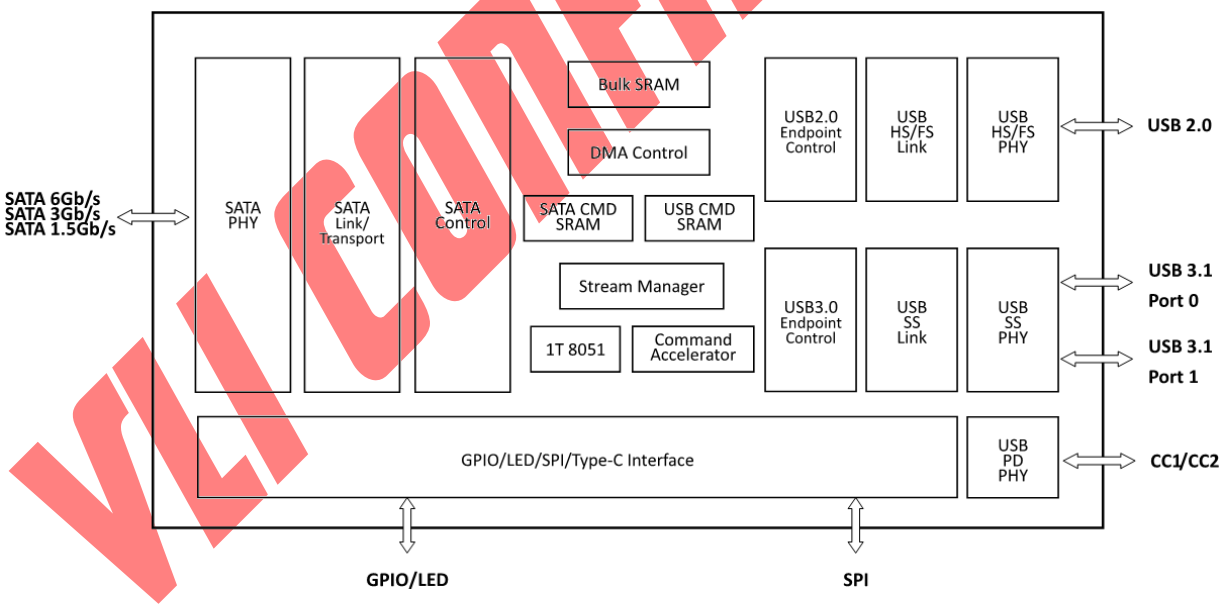
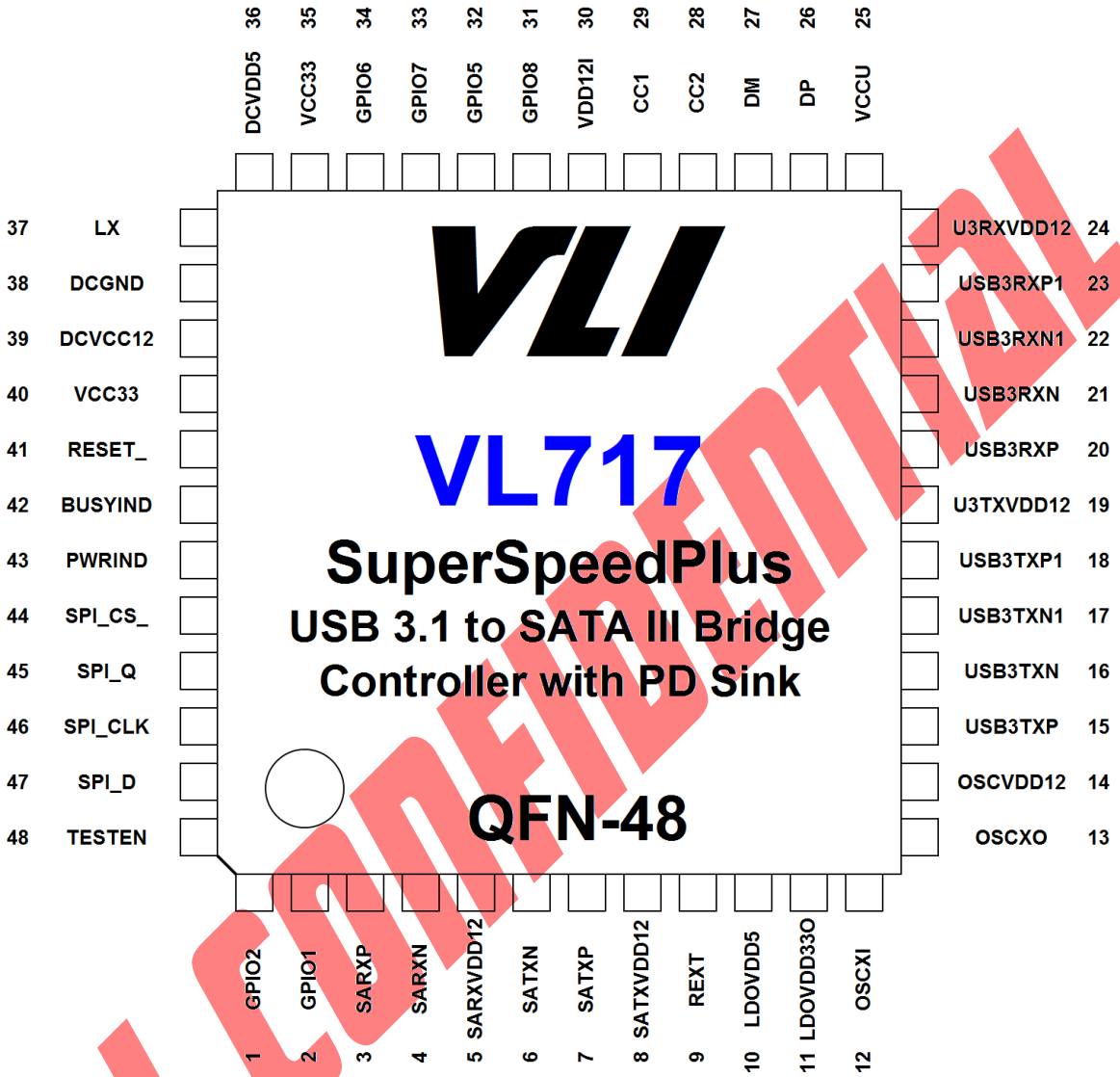


Figure 1 – VL717 Block Diagram

Pinout



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Figure 2 – VL717 QFN-48 Pin Diagram

Pin List

Table 1 – VL717 QFN-48 Pin List

Pin	Pin Name	Pin	Pin Name
1	GPIO2	25	VCCU
2	GPIO1	26	DP
3	SARXP	27	DM
4	SARXN	28	CC2
5	SARXVDD12	29	CC1
6	SATXN	30	VDD12I
7	SATXP	31	GPIO8
8	SATXVDD12	32	GPIO5
9	REXT	33	GPIO7
10	LDOVDD5	34	GPIO6
11	LDOVDD33O	35	VCC33
12	OSCXI	36	DCVDD5
13	OSCXO	37	LX
14	OSCVDD12	38	DCGND
15	USB3TXP	39	DCVCC12
16	USB3TXN	40	VCC33
17	USB3TXN1	41	RESET_
18	USB3TXP1	42	BUSYIND
19	U3TXVDD12	43	PWRIND
20	USB3RXP	44	SPI_CS_
21	USB3RXN	45	SPI_Q
22	USB3RXN1	46	SPI_CLK
23	USB3RXP1	47	SPI_D
24	U3RXVDD12	48	TESTEN

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Pin Descriptions

Signal Type Definition

Name	Type	Signal Description
Input	I	A standard input-only signal
Output	O	A standard active driver
Input/Output	I/O	A bi-directional signal
Analog bias	A_{BIAS}	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network
Power	PWR	A power pin
Ground	GND	A ground pin

Serial ATA Interface

Pin Name	QFN48	I/O	Signal Description
SARXP	3	I	SATA Port Differential Receive Data +
SARXN	4	I	SATA Port Differential Receive Data -
SATXP	7	O	SATA Port Differential Transmit Data +
SATXN	6	O	SATA Port Differential Transmit Data -
SATXVDD12	8	PWR	Analog 1.2V
SARXVDD12	5	PWR	Analog 1.2V

USB 3.1 Interface

Pin Name	QFN48	I/O	Signal Description
USB3RXP	20	I	USB 3.1 Port0 Differential Receive Data +
USB3RXN	21	I	USB 3.1 Port0 Differential Receive Data -
USB3TXP	15	O	USB 3.1 Port0 Differential Transmit Data +
USB3TXN	16	O	USB 3.1 Port0 Differential Transmit Data -
USB3RXP1	23	I	USB 3.1 Port1 Differential Receive Data +
USB3RXN1	22	I	USB 3.1 Port1 Differential Receive Data -
USB3TXP1	18	O	USB 3.1 Port1 Differential Transmit Data +
USB3TXN1	17	O	USB 3.1 Port1 Differential Transmit Data -
U3RXVDD12	24	PWR	Analog 1.2V
U3TXVDD12	19	PWR	Analog 1.2V

USB 2.0 Interface

Pin Name	QFN48	I/O	Signal Description
DP	26	I/O	USB 2.0 Bus Data Plus (D+)
DM	27	I/O	USB 2.0 Bus Data Minus (D–)
VCCU	25	PWR	Analog 3.3V

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USB Type-C & PD Interface

Pin Name	QFN48	I/O	Signal Description
CC1	29	I/O	Configuration Channel 1, built-in Rd resistor (5.1 kΩ ± 20%)
CC2	28	I/O	Configuration Channel 2, built-in Rd resistor (5.1 kΩ ± 20%)

Serial EEPROM Interface

Pin Name	QFN48	I/O	Signal Description
SPI_CS_	44	O	Serial Flash Chip Enable
SPI_D	47	O	Serial Flash Data Input
SPI_Q	45	I	Serial Flash Data Output
SPI_CLK	46	O	Serial Flash Clock

Analog Command Block

Pin Name	QFN48	I/O	Signal Description
OSCXI	12	I	25M crystal input
OSCXO	13	O	25M crystal output
REXT	9	A_{BIAS}	Connect to external resistor
LDOVDD5	10	PWR	5.0V voltage input for 5V to 3.3V LDO
LDOVDD33O	11	O	3.3V voltage output for 5V to 3.3V LDO
DCVDD5	36	PWR	5.0V voltage input for DC2DC regulator
LX	37	O	1.2V voltage output for DC2DC regulator
DCGND	38	GND	Ground for DC2DC regulator
DCVCC12	39	PWR	1.2V voltage input for core power
OSCVDD12	14	PWR	Oscillator analog 1.2V

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General Purpose I/O and Miscellaneous

Pin Name	QFN48	I/O	Signal Description
BUSYIND	42	O	Busy LED Indicator, including PWM Typical Low Level Output Current I_{OL} = 22.6mA @ 0.4V (max); Typical High Level Output Current I_{OH} = 39.6mA @ 2.4V (min)
PWRIND	43	O	Power LED Indicator, including PWM Typical Low Level Output Current I_{OL} = 22.6mA @ 0.4V (max); Typical High Level Output Current I_{OH} = 39.6mA @ 2.4V (min)
RESET_	41	I	External Chip Reset
GPIO_1	2	I/O	General Purpose I/O (I_{OL} = 22.6mA @ 0.4V; I_{OH} = 39.6mA @ 2.4V in output mode) Default: Device power down control
GPIO_2	1	I/O	General Purpose I/O, including PWM (I_{OL} = 22.6mA @ 0.4V; I_{OH} = 39.6mA @ 2.4V in output mode) Default: USB 3.1/USB2.0 mode indicator
GPIO_5	32	I/O	General Purpose I/O (I_{OL} = 22.6mA @ 0.4V; I_{OH} = 39.6mA @ 2.4V in output mode) Default: Push button trigger pin
GPIO_6	34	I/O	General Purpose I/O (I_{OL} = 22.6mA @ 0.4V; I_{OH} = 39.6mA @ 2.4V in output mode) Default: USB cable power detect
GPIO_7	33	I/O	General Purpose I/O, including PWM (I_{OL} = 22.6mA @ 0.4V; I_{OH} = 39.6mA @ 2.4V in output mode) Default: Device write protect control
GPIO_8	31	I/O	General Purpose I/O (I_{OL} = 22.6mA @ 0.4V; I_{OH} = 39.6mA @ 2.4V in output mode) Default: Push button status indicator

Test Pin

Pin Name	QFN48	I/O	Signal Description
TESTEN	48	I	Test Mode Enable Do not connect for normal operation. Internal pull down

Power and Ground

Pin Name	QFN48	I/O	Signal Description
VCC33	35, 40	PWR	Digital IO power 3.3V
VDD12I	30	PWR	Digital Core power 1.2V

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Electrical Specification

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-55	125	°C	—
T_A	Ambient Temperature	0	70	°C	—
V_{DD33}	Power Supply Voltage	-0.5	3.69	V	—
V_{DD50}	Input Voltage	-0.5	5.5	V	—
V_O	Output Voltage at any output	-0.5	VCC+ 0.5	V	—
V_{ESD}	Electrostatic Discharge	—	2	kV	Human Body Model

Note: Stress above conditions may cause permanent damage to the device.
Functional operation of this device should be restricted to the conditions described.

Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC33}	Digital IO power 3.3V	3.0	3.3	3.6	V
LDOVDD5	5V to 3.3V LDO 5V Power Input	4.5	5	5.5	V
DCVDD5	5V to 1.2V DC2DC 5V Power Input	4.5	5	5.5	V
V_{DD12I}	Digital Core power 1.2V	1.08	1.2	1.26	V
DGND	Ground	—	0	—	V

General IO DC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.30	0.8	V	—
V_{IH}	Input High Voltage	2.0	3.6	V	—
V_{OL}	Output Low Voltage	—	0.4	V	IOL=15.8mA
V_{OH}	Output High Voltage	2.4	—	V	IOH=26.5mA
I_{IL}	Input Leakage Current	—	+/-10	µA	0<VIN<VCC
I_{OZ}	Tristate Leakage Current	—	+/-10	µA	0<VOUT<VCC

Internal 5V to 1.2V DC/DC Converter

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	4.5	5.0	5.5	V	
Output Voltage	1.14	1.2	1.26	V	
Max. Output Current		450	520	mA	
Output Voltage Tolerance		+/- 5%			

Internal 5V to 3.3V LDO Regulator

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	4.5	5.0	5.5	V	
Output Voltage	3.135	3.3	3.465	V	
Max. Output Current		50	100	mA	
Output Voltage Tolerance		+/- 5%			

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External Crystal Electrical Characteristics

Please refer to the Figure 3.

Symbol	Parameter	Min	Typ	Max	Unit
FL	Normal Frequency		25		MHz
	Oscillation Mode		Fundamental		
	Frequency Tolerance	-30		30	ppm
	Aging	-5		5	ppm
CL	Loading Capacitance		12		pf
C0	Shunt Capacitance	1	3	7	pf
Rr	Effective Resistance			50	ohms

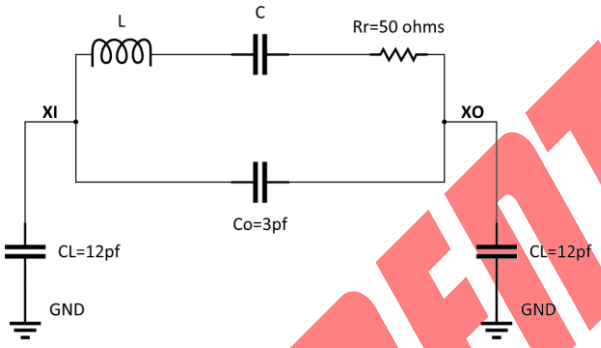
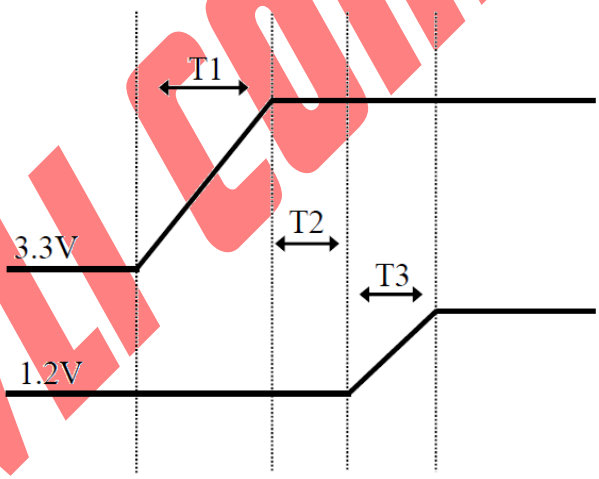


Figure 3 – 25MHz Crystal equivalent circuit and spec requirement

VL717 Built-in Regulator Power Sequence



Time	Min	Max
T1	~	14ms
T2	0	2ms
T3	~	1.6ms

Note: Based on Vbus rising time = 20ms

VL717 power sequence is Vbus -> 3.3V -> 1.2V.
Built-in 3.3V regulator is activated when Vbus is reaching 0.8V.

T1: 3.3V Rising time (0%-100%)
T2: Time interval between 3.3V and 1.2V
T3: 1.2V Rising time (0%-100%)

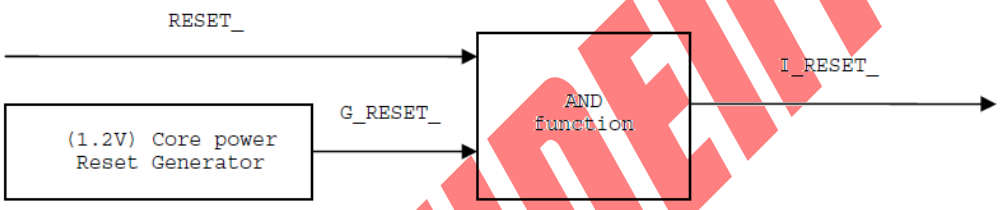
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VL717 Reset Scheme

There are two sources of generating VL717 reset signal: One is from external reset (RESET_), the other is from the internal power-on reset (G_RESET_). The AND function of these two signals generates digital circuit reset signal (I_RESET_) as in below diagram.

G_RESET_ will assert low level voltage when the core power is under 0.9V. When the core power rises to 0.9V, it will keep low in the period of 1 mini second, then logically de-asserted. When The I_RESET_ becomes logic-1, the internal logic will wait for extra 20 mini seconds, then begin to work. The extra 20 mini seconds will cover the T3 period to make sure the 1.2V is stable.

Since VL717 has its own internal power-on reset signal G_RESET_, external reset is optional and can be tied to 3.3V for BOM cost consideration. When external reset circuit is implemented, RESET_ pin must be de-asserted within 40 mini seconds from Vbus is ready.



PD BMC DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
$V_{BMCSWING}$	Voltage Swing	1.05	1.2	V	—
Z_{BMCDRV}	Drive Output Resistance	33	75	Ω	—
T_{BMCR}	Rise Time	300		ns	—
T_{BMCF}	Fall Time	300		ns	—

USB Full Speed DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{FSIH}	Full-speed Input High	2.0		V	—
V_{FSIL}	Full-speed Input Low		0.8	V	—
V_{FSCM}	Differential Common Mode Voltage	0.8	2.5	V	—
V_{FSOL}	Full-speed Output Low	0.0	0.3	V	—
V_{FSOH}	Full-speed Output High	2.8	3.6	V	—
T_{FSR}	Full-speed Rise Time	4	20	ns	—
T_{FSF}	Full-speed Fall Time	4	20	ns	—
V_{FSCRS}	Full-speed Output Signal Crossover Voltage	1.3	2.0	V	—

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USB High Speed DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{HSSQ}	High-speed squelch detection threshold	100	150	mV	—
V_{HSCM}	High-speed data signaling common mode voltage	-50	500	mV	—
V_{HSOI}	High-speed idle level	-10	10	mV	—
V_{HSOH}	High-speed data high	360	440	mV	—
V_{HSOL}	High-speed data low	-10	10	mV	—
V_{CHIRPJ}	Chirp J level	700	1100	mV	—
V_{CHIRPK}	Chirp K level	-900	-500	mV	—
Z_{HSDRV}	Drive output resistance	40.5	49.5	Ω	—
T_{HSR}	High-speed Rise Time	500		ps	—
T_{HSF}	High-speed Fall Time	500		ps	—

USB 3.1 Gen2 TX Characteristics (10 GT/s)

Symbol	Parameter	Min	Max	Unit	Note
$V_{TX-DIFF-PP}$	Differential p-p Tx swing	0.8	1.2	V	—
$V_{TX-DE-RATIO}$	Tx de-emphasis	2.1	4.1	dB	—
$V_{TX-PRE-RATIO}$	Tx pre-shoot	1.2	3.2	dB	—
$R_{TX-DIFF-DC}$	DC differential impedance	72	120	Ω	—
$V_{TX-RCV-DETECT}$	The Voltage Change allowed during Receiver Detection		0.6	V	—
T_{TX-EYE}	Transmitter Eye	0.646		UI	—
$T_{TX-DJ-DD}$	Tx Deterministic Jitter		0.170	UI	—
$C_{TX-PARASITIC}$	Tx input capacitance for return loss		1.1	pF	
R_{TX-DC}	Transmitter DC Common Mode Impedance	18	30	Ω	—
$V_{TX-DC-CM}$	Transmitter DC Common Mode Voltage	0	2.2	V	—
$V_{TX-CM-AC-PP-ACTIVE}$	Tx AC Common Mode Voltage Active		100	mV	—
$V_{TX-IDLE-DIFF-AC-pp}$	Electrical Idle Differential P-P Output Voltage	0	10	mV	—
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Output Voltage	0	10	mV	—

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USB 3.1 Gen2 RX Characteristics (10 GT/s)

Symbol	Parameter	Min	Max	Unit	Note
UI	Unit Interval	99.97	100.03	ps	UI does not account for SSC caused variations
R_{RX-DC}	Receiver DC common mode impedance	18	30	Ω	DC impedance limits are needed to guarantee Receiver detect Measured with respect to ground over a voltage of 500mV maximum
$R_{RX-DIFF-DC}$	DC differential impedance	72	120	Ω	
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input CM Input Impedance for V>0 during Reset or power down	25k		Ω	Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 – 500mv with respect to ground
$V_{RX-LFPS-DET-DIFF_{p-p}}$	LFPS Detect Threshold	100	300	mV	Below the minimum is noise Must wake up above the maximum
$V_{RX-DIFF-PP-POST-EQ}$	Differential Rx peak-to-peak voltage	30		mV	Measured after the Rx EQ function (Section 6.8.2)
t_{RX-TJ}	Max Rx inherent timing error		0.394	UI	Measured after the Rx EQ function (Section 6.8.2)
$t_{RX-DJ-DD}$	Max Rx inherent deterministic timing error		0.21	UI	Maximum Rx inherent deterministic timing error
$C_{RX-PARASITIC}$	Rx input capacitance for return loss		1.0	pF	
$V_{RX-CM-AC-P}$	Rx AC common mode voltage		150	mV Peak	Measured at Rx pins into a pair of 50Ω terminations into ground Includes Tx and channel conversion, AC range up to 5 GHz
$V_{RX-CM-DC-ACTIVE-IDLE-DELTA-P}$	Rx AC common mode voltage during the U1 to U0 transition		200	mV Peak	Measured at Rx pins into a pair of 50Ω terminations into ground Includes Tx and channel conversion, AC range up to 5 GHz

USB 3.1 Gen 1 TX Characteristics (5 GT/s)

Symbol	Parameter	Min	Max	Unit	Note
$V_{TX-DIFF-PP}$	Differential p-p Tx swing	0.8	1.2	V	—
$V_{TX-DE-RATIO}$	Tx de-emphasis	3.0	4.0	dB	—
$R_{TX-DIFF-DC}$	DC differential impedance	72	120	Ω	—
$V_{TX-RCV-DETECT}$	The Voltage Change allowed during Receiver Detection		0.6	V	—
T_{TX-EYE}	Transmitter Eye	0.625		UI	—
$T_{TX-DJ-DD}$	Tx Deterministic Jitter		0.205	UI	—
R_{TX-DC}	Transmitter DC Common Mode Impedance	18	30	Ω	—
$V_{TX-DC-CM}$	Transmitter DC Common Mode Voltage	0	2.2	V	—
$V_{TX-CM-AC-PP-ACTIVE}$	Tx AC Common Mode Voltage Active		100	mV	—
$V_{TX-IDLE-DIFF-AC-pp}$	Electrical Idle Differential P-P Output Voltage	0	10	mV	—
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Output Voltage	0	10	mV	—

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USB 3.1 Gen 1 RX Characteristics (5.0 GT/s)

Symbol	Parameter	Min	Max	Unit	Note
UI	Unit Interval	199.94	200.06	ps	UI does not account for SSC caused variations
R_{RX-DC}	Receiver DC common mode impedance	18	30	Ω	DC impedance limits are needed to guarantee Receiver detect Measured with respect to ground over a voltage of 500mV maximum
$R_{RX-DIFF-DC}$	DC differential impedance	72	120	Ω	
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input CM Input Impedance for V>0 during Reset or power down	25k		Ω	Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 – 500mv with respect to ground
$V_{RX-LFPS-DET-DIFF_{p-p}}$	LFPS Detect Threshold	100	300	mV	Below the minimum is noise Must wake up above the maximum
$V_{RX-DIFF-PP-POST-EQ}$	Differential Rx peak-to-peak voltage	30		mV	Measured after the Rx EQ function (Section 6.8.2)
t_{RX-TJ}	Max Rx inherent timing error		0.45	UI	Measured after the Rx EQ function (Section 6.8.2)
$t_{RX-DJ-DD}$	Max Rx inherent deterministic timing error		0.3	UI	Maximum Rx inherent deterministic timing error
$C_{RX-PARASITIC}$	Rx input capacitance for return loss		1.1	pf	
$V_{RX-CM-AC-P}$	Rx AC common mode voltage		150	mV Peak	Measured at Rx pins into a pair of 50Ω terminations into ground Includes Tx and channel conversion, AC range up to 5 GHz
$V_{RX-CM-DC-ACTIVE-IDLE-DELTA-P}$	Rx AC common mode voltage during the U1 to U0 transition		200	mV Peak	Measured at Rx pins into a pair of 50Ω terminations into ground Includes Tx and channel conversion, AC range up to 5 GHz

SATA TX Characteristics

Symbol	Parameter	Min	Max	Unit	Note
Z_{diffTX}	TX Pair Differential Impedance	85	115	Ohm	
Z_{s-eTX}	TX Single-Ended Impedance	40			
$RL_{DD11,TX}$	TX Differential Mode Return Loss (150MHz-300MHz)	14		dB	
	TX Differential Mode Return Loss (300MHz-600MHz)	8		dB	
	TX Differential Mode Return Loss (600MHz-1.2GHz)	6		dB	
	TX Differential Mode Return Loss (1.2GHz-2.4GHz)	6		dB	
	TX Differential Mode Return Loss (2.4GHz-3.0GHz)	3		dB	
	TX Differential Mode Return Loss (3.0GHz-5.0GHz)	1		dB	Only for Gen2i
$RL_{DD11,TX}$	TX Differential Mode Return Loss Start for slope for Gen3	Min at 300MHz is 14		dB	
	Slope of TX Differential Mode Return Loss for Gen3	-13		dB/dec	

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	TX Differential Mode Return Loss Max Frequency for Gen3		Max is 3	GHz	
$RL_{CC11,TX}$	TX Common Mode Return Loss (150MHz-300MHz)	8		dB	
	TX Common Mode Return Loss (300MHz-600MHz)	5		dB	
	TX Common Mode Return Loss (600MHz-1.2GHz)	2		dB	
	TX Common Mode Return Loss (1.2GHz-2.4GHz)	1		dB	
	TX Common Mode Return Loss (2.4GHz-3.0GHz)	1		dB	
	TX Common Mode Return Loss (3.0GHz-5.0GHz)	1		dB	Only for Gen2i
$RL_{DC11,TX}$	TX Impedance Balance (150MHz-300MHz)	30		dB	
	TX Impedance Balance (300MHz-600MHz)	20		dB	
	TX Impedance Balance (600MHz-1.2GHz)	10		dB	
	TX Impedance Balance (1.2GHz-2.4GHz)	10		dB	
	TX Impedance Balance (2.4GHz-3.0GHz)	4/10		dB	For Gen3i is 10dB
	TX Impedance Balance (3.0GHz-5.0GHz)	4		dB	
	TX Impedance Balance (5.0GHz-6.5GHz)	4			Only for Gen3i
V_{diffTX}	TX Differential Output Voltage	400	600	mVppd	For Gen1
	TX Differential Output Voltage	400	700	mVppd	For Gen2
	TX Differential Output Voltage	200	900	mVppd	For Gen3
UI_{VminTX}	TX Minimum Voltage Measurement Interval	0.45	0.55	UI	
$t_{20\text{-}80TX}$	TX Rise/Fall Time	100	273	ps	For Gen1
	TX Rise/Fall Time	67	136	ps	For Gen2
	TX Rise/Fall Time	33	80	ps	For Gen3
t_{skewTX}	TX Differential Skew		20	ps	
$V_{cm,acTX}$	TX AC Common Mode Voltage		50	mVp-p	
	TX AC Common Mode Voltage 3 GHz Max		26	dBmV(rms)	For Gen3
	TX AC Common Mode Voltage 6 GHz Max		30	dBmV(rms)	For Gen3
$D_{vdiffOOB}$	OOB Differential Delta		25	mV	
D_{vcmOOB}	OOB Common Mode Delta		50	mV	
R/F_{bal}	TX Rise/Fall Imbalance		20	%	Only for Gen2
Amp_{bal}	TX Amplitude Imbalance		30	%	Only for Gen2
	TJ at Connector Clk-Data fBAUD/500 JTF Defined		0.37	UI	For Gen1/Gen2
	DJ at Connector Clk-Data fBAUD/500 JTF Defined		0.19	UI	For Gen1/Gen2
	Jitter Transfer Function Bandwidth (D24.3,high pass -3dB)	1.1	3.1	MHz	For Gen1/Gen2
	Jitter Transfer Function Peaking		3.5	dB	For Gen1/Gen2
	Jitter Transfer Function Low Frequency Attenuation	69	75	db	For Gen1/Gen2
	Jitter Transfer Function Bandwidth (D24.3,high pass -3dB)	2.2	6.2	MHz	For Gen3
	Jitter Transfer Function Peaking		3.5	dB	For Gen3
	Jitter Transfer Function Low Frequency Attenuation	35.2	41.2	db	For Gen3
	TJ(10-12)before and after CIC,Clk-Data JTF Defined		0.52	UI	For Gen3
	TJ(10-6)before and after CIC,Clk-Data JTF Defined		0.46	UI	For Gen3

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SATA RX Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{diffRX}	Gen1 RX Differential Input Voltage	240	600	mVppd	
	Gen2 RX Differential Input Voltage	240	750		
	Gen3 RX Differential Input Voltage	240	1000		
$t_{20\text{-}80RX}$	Gen1 RX Rise/Fall time	100	273	ps	
	Gen2 RX Rise/Fall time	67	136		
	Gen2 RX Rise/Fall time	62	75		
t_{skewRX}	Gne2 RX Differential Skew		50	Ps	
	Gen3 RX Differential Skew		30		
$V_{cm,\ acRX}$	RX AC Common Mode Voltage		100	mVppd	
$f_{cm,\ acRX}$	RX AC Common Mode Frequency	2	200	MHz	
	Gen1 TJ at Connector, Data-Data, 5UI		0.43	UI	
	Gen1 DJ at Connector, Data-Data, 5UI		0.25	UI	
	Gen1 TJ at Connector, Data-Data, 250UI		0.6	UI	
	Gen1 TJ at Connector, Data-Data, 250UI		0.35	UI	
	Gen2 TJ at Connector, Clk-Data, $f_{BAUD}/10$		0.46	UI	
	Gen2 DJ at Connector, Clk-Data, $f_{BAUD}/10$		0.35	UI	
	Gen2 TJ at Connector, Clk-Data, $f_{BAUD}/500$		0.60	UI	
	Gen2 DJ at Connector, Clk-Data, $f_{BAUD}/500$		0.42	UI	
Gen3 TJ after CIC	Clk-Data JTF Defined		0.60	UI	
Gen3 RJ before CIC	MFTP Clk-Data JTF Defined		0.60		
Z_{diffRX}	RX Pair Differential Impedance	85	115	Ohm	
$Z_{s\text{-}eRX}$	RX single-ended Impedance	40		Ohm	
$RL_{DD11,RX}$	Gen2i/m RX Differential Mode Return Loss (150MHz-300MHz)	18		dB	
	Gen2i/m RX Differential Mode Return Loss (300MHz-600MHz)	14		dB	
	Gen2i/m RX Differential Mode Return Loss (600MHz-1.2GHz)	10		dB	
	Gen2i/m RX Differential Mode Return Loss (1.2GHz-2.4GHz)	8		dB	
	Gen2i/m RX Differential Mode Return Loss (2.4GHz-3.0GHz)	3		dB	
	Gen2i/m RX Differential Mode Return Loss (3.0GHz-5.0GHz)	1		dB	
	Gen3i RX Differential Mode Return Loss (min @ 300MHz)	18		dB	
	Gen3i Slop of RX Differential Mode Return Loss	-13		dB/dec	
	Gen3i RX Differential Mode Return Loss max frequency		6.0	GHz	
RL_{CC11}	Gen2i/m RX Common Mode Return Loss (150MHz-300MHz)	5		dB	
	Gen2i/m RX Common Mode Return Loss (300MHz-600MHz)	5		dB	

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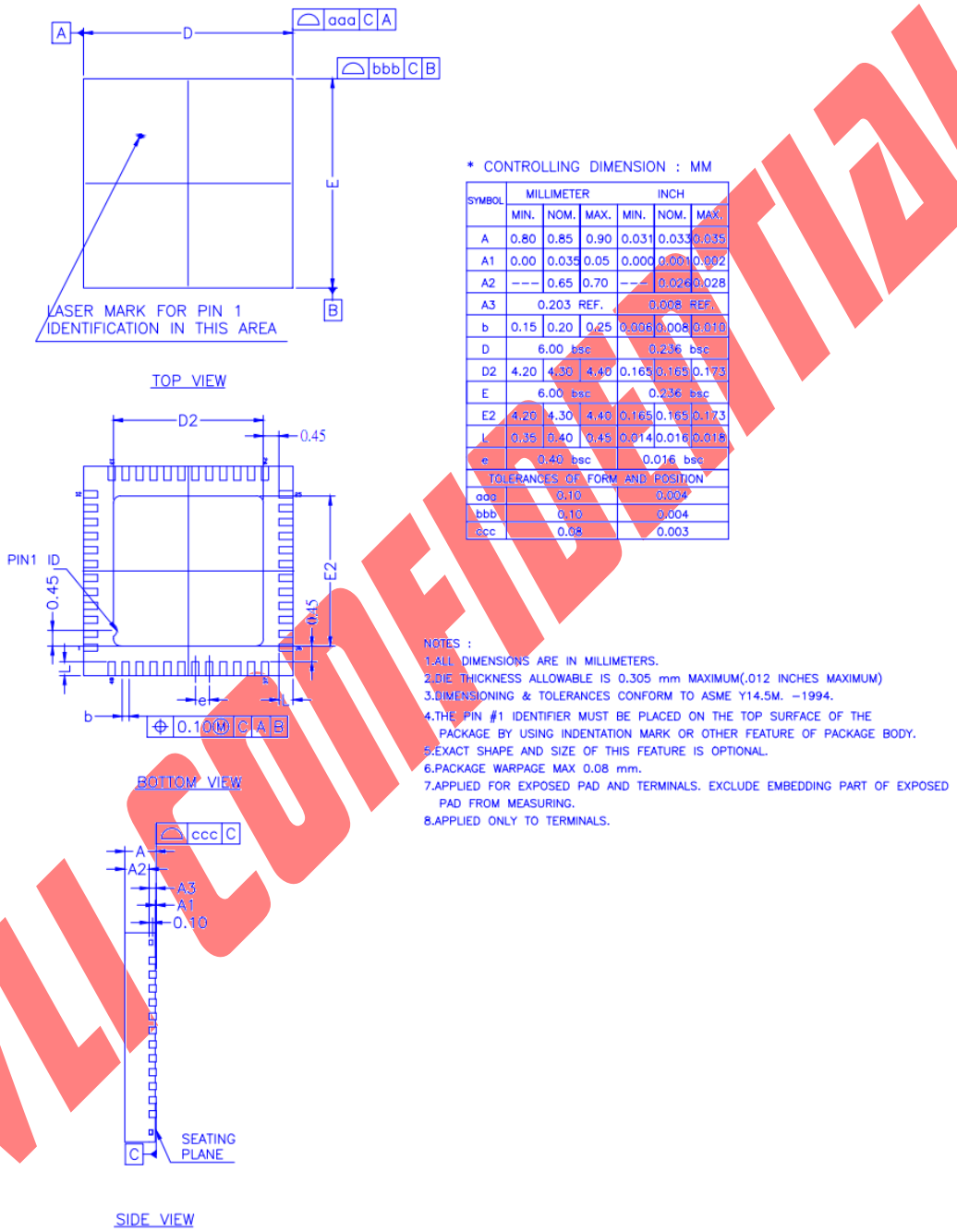
	Gen2i/m RX Common Mode Return Loss (600MHz-1.2GHz)	2		dB
	Gen2i/m RX Common Mode Return Loss (1.2GHz-2.4GHz)	1		dB
	Gen2i/m RX Common Mode Return Loss (2.4GHz-3.0GHz)	1		dB
	Gen2i/m RX Common Mode Return Loss (3.0GHz-5.0GHz)	1		dB
V_{thresh}	Gen1 OOB Signal Detection Threshold	50	200	mVppd
	Gen2/3 OOB Signal Detection Threshold	75	200	mVppd
UI_{OOB}	UI During OOB Signaling	646.67	686.67	ps
	COMINIT/COMRESET/COMWAKE Transmit Burst Length	160	160	UI_{OOB}
	COMINIT/COMRESET Transmit Gap Length	480	480	UI_{OOB}
	COMWAKE Transmit Gap Length	160	160	UI_{OOB}
	COMWAKE Gap Detection Window	55	175	ns
	COMINIT/COMRESET Gap Detection Window	175	525	ns

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Package Mechanical Specifications

QFN-48 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	seconds



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.035	0.05	0.000	0.001	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.00 bsc			0.236 bsc		
D2	4.20	4.30	4.40	0.165	0.169	0.173
E	6.00 bsc			0.236 bsc		
E2	4.20	4.30	4.40	0.165	0.169	0.173
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.40 bsc			0.016 bsc		
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.08			0.003		

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Figure 4 – QFN 48L 6x6x0.85 mm Mechanical Specification

Package Top Side Marking

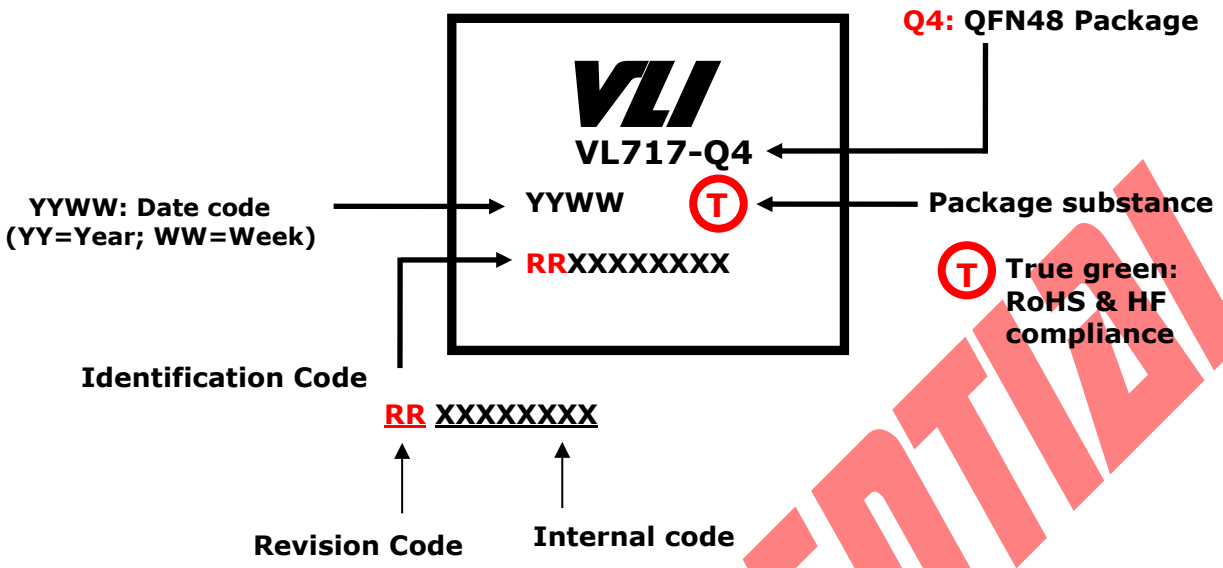


Figure 5 – VL717 Package Top Side Marking

Ordering Information

Please contact VIA Labs sales representative or distributor in your region for ordering part number details.

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