CP2104

SINGLE-CHIP USB-TO-UART BRIDGE

For newer designs, the CP2102N devices offer compatible footprints and are recommended for use instead of the CP2104. See the Silicon Labs website (www.silabs.com/usbxpress) for more information.

Single-Chip USB to UART Data Transfer

- Integrated USB transceiver; no external resistors required
- Integrated clock; no external crystal required
- Integrated 1024-Byte One-Time Programmable ROM for customizable product information
- On-chip power-on reset circuit
- On-chip voltage regulator: 3.45 V output

USB Function Controller

- USB Specification 2.0 compliant; full-speed (12 Mbps)
- USB Suspend states supported via SUSPEND and SUSPEND pins

Asynchronous Serial Data BUS (UART)

- All handshaking and modem interface signals
- Data formats supported:
  - Data bits: 5, 6, 7, and 8
  - Stop bits: 1, 1.5, and 2
  - Parity: odd, even, mark, space, no parity
- Baud rates: 300 bps to 2 Mbits
- 576 byte receive buffer; 576 byte transmit buffer
- Hardware or X-On/X-Off handshaking supported
- Four GPIO signals for status and control
- Configurable I/O (1.8 V to V_{DD}) using V_{IO} pin
- Configurable I/O (V_{DD} to 5 V) using external pull-up
- RS-485 mode with bus transceiver control

Virtual COM Port Device Drivers

- Works with Existing COM Port PC Applications
- Royalty-Free Distribution License
- Windows 7®/Vista®/XP®/Server 2003®/2000®
- Mac® OS-X
- Linux®

USBXpress™ Direct Driver Support

- Royalty-Free Distribution License
- Windows 7/Vista/XP/Server 2003/2000
- Windows CE® 6.0, 5.0, and 4.2

Example Applications

- Upgrade of RS-232 legacy devices to USB
- Upgrade of RS-485 legacy devices to USB
- Cellular phone USB interface cable
- PDA USB interface cable
- USB to RS-232 serial adapter

Supply Voltage

- Self-powered: 3.0 to 3.6 V
- USB bus powered: 4.0 to 5.25 V
- I/O voltage: 1.8 V to V_{DD}

Package

- RoHS-compliant 24-pin QFN (4x4 mm)

Ordering Part Number

- CP2104-F03-GM

Temperature Range: –40 to +85 °C

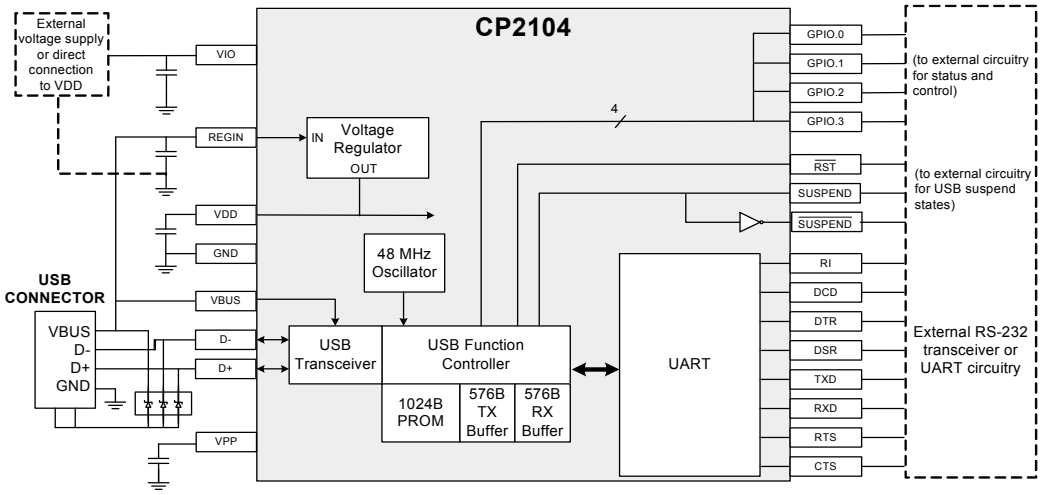


Figure 1. Example System Diagram

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1. System Overview

The CP2104 is a highly-integrated USB-to-UART Bridge Controller providing a simple solution for updating RS-232/RS-485 designs to USB using a minimum of components and PCB space. The CP2104 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, one-time programmable ROM, and asynchronous serial data bus (UART) with full modem control signals in a compact 4 x 4 mm QFN-24 package (sometimes called “MLF” or “MLP”). No other external USB components are required.

The on-chip one-time programmable ROM may be used to customize the USB Vendor ID, Product ID, Product Description String, Power Descriptor, Device Release Number, Device Serial Number, and GPIO configuration as desired for OEM applications.

Royalty-free Virtual COM Port (VCP) device drivers provided by Silicon Labs allow a CP2104-based product to appear as a COM port to PC applications. The CP2104 UART interface implements all RS-232/RS-485 signals, including control and handshaking signals, so existing system firmware does not need to be modified. The device also features up to four GPIO signals that can be user-defined for status and control information. Support for I/O interface voltages down to 1.8 V is provided via a V_{IO} pin. In many existing RS-232 designs, all that is required to update the design from RS-232 to USB is to replace the RS-232 level-translator with the CP2104. Direct access driver support is available through the Silicon Labs USBXpress driver set. See www.siliconlabs.com for the latest application notes and product support information for the CP2104.

An evaluation kit for the CP2104 (Part Number: CP2104EK) is available. It includes a CP2104-based USB-to-UART/RS-232 evaluation board, a complete set of VCP device drivers, USB and RS-232 cables, and full documentation. Contact a Silicon Labs sales representatives or go to www.siliconlabs.com to order the CP2104 Evaluation Kit.

2. Electrical Characteristics

Table 1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Ambient Temperature Under Bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on $\overline{RST}$, GPIO or UART Pin with respect to GND	$V_{IO} \geq 2.2$ V $V_{IO} < 2.2$ V	–0.3 –0.3	— —	5.8 V_{IO} + 3.6	V
Voltage on VBUS with respect to GND	$V_{DD} \geq 3.0$ V V_{DD} not powered	–0.3 –0.3	— —	5.8 V_{DD} + 3.6	V
Voltage on V_{DD} or V_{IO} with respect to GND		–0.3	—	4.2	V
Maximum Total Current through V_{DD}, V_{IO}, and GND		—	—	500	mA
Maximum Output Current Sunk by $\overline{RST}$ or any I/O pin		—	—	100	mA

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at or exceeding the conditions in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Global DC Electrical Characteristics

V_{DD} = 3.0 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Voltage (V_{DD})		3.0	—	3.6	V
Digital Port I/O Supply Voltage (V_{IO})		1.8	—	V_{DD}	V
Voltage on V_{PP} with respect to GND during a ROM programming operation	$V_{IO} \geq 3.3$ V	5.75	—	V_{IO} + 3.6	V
Capacitor on V_{PP} for ROM programming		—	4.7	—	µF
Supply Current[1]	Normal Operation; V_{REG} Enabled	—	17.0	18.5	mA
Supply Current[1]	Suspended; V_{REG} Enabled	—	100	200	µA
Supply Current—USB Pull-up[2]		—	200	228	µA
Specified Operating Temperature Range		–40	—	+85	°C

Notes:
1. If the device is connected to the USB bus, the USB Pull-up Current should be added to the supply current for total supply current.
2. The USB Pull-up supply current values are calculated values based on USB specifications.

Table 3. UART and Suspend I/O DC Electrical Characteristics

V_{DD} = 3.0 to 3.6 V, V_{IO} = 1.8 V to V_{DD}, –40 to +85 °C unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	UNITS
Output High Voltage (V_{OH})	I_{OH} = –10 µA I_{OH} = –3 mA I_{OH} = –10 mA	V_{IO} – 0.1 V_{IO} – 0.2 —	— — V_{IO} – 0.4	— — —	V
Output Low Voltage (V_{OL})	I_{OL} = 10 µA I_{OL} = 8.5 mA I_{OL} = 25 mA	— — —	— — 0.6	0.1 0.4 —	V
Input High Voltage (V_{IH})		0.7 x V_{IO}	—	—	V
Input Low Voltage (V_{IL})		—	—	0.6	V
Input Leakage Current	Weak Pull-Up Off Weak Pull-Up On, V_{IN} = 0 V	— —	— 25	1 50	µA
Maximum Input Voltage	Open drain, logic high (1)	—	—	5.8	V

Table 4. Reset Electrical Characteristics

–40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
$\overline{RST}$ Input High Voltage		0.75 x V_{IO}	—	—	V
$\overline{RST}$ Input Low Voltage		—	—	0.6	V
Minimum $\overline{RST}$ Low Time to Generate a System Reset		15	—	—	µs
V_{DD} Ramp Time for Power On		—	—	1	ms

Table 5. Voltage Regulator Electrical Specifications

–40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Range		3.0	—	5.25	V
Output Voltage	Output Current = 1 to 100 mA*	3.3	3.45	3.6	V
VBUS Detection Input Threshold		2.5	—	—	V
Bias Current		—	—	120	µA
***Note:** The maximum regulator supply current is 100 mA. This includes the supply current of the CP2104.					

Table 6. GPIO Output Specifications

–40 to +85 °C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
RS-485 Active Time After Stop Bit		—	1	—	bit time*
TX Toggle Rate		—	10	—	Hz
RX Toggle Rate		—	10	—	Hz
***Note:** Bit-time is calculated as 1 / baud rate.					

3. Pinout and Package Definitions

Table 7. CP2104 Pin Definitions

Name	Pin #	Type	Description
V_{DD}	6	Power In Power Out	Power Supply Voltage Input. Voltage Regulator Output. See Section 9.
V_{IO}	5	Power In	I/O Supply Voltage Input.
GND	2		Ground. Must be tied to ground.
$\overline{RST}$	9	D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for the time specified in Table 4.
REGIN	7	Power In	5 V Regulator Input. This pin is the input to the on-chip voltage regulator.
VBUS	8	D In	VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network.
V_{PP}	16*	Special	Connect a 4.7 µF capacitor between this pin and ground to support ROM programming via USB interface.
D+	3	D I/O	USB D+
D–	4	D I/O	USB D–
TXD	21	D Out	Asynchronous data output (UART Transmit)
RXD	20	D In	Asynchronous data input (UART Receive)
CTS	18*	D In	Clear to Send control input (active low)
RTS	19*	D Out	Ready to Send control output (active low)
DSR	22*	D In	Data Set Ready control input (active low)
DTR	23*	D Out	Data Terminal Ready control output (active low)
DCD	24*	D In	Data Carrier Detect control input (active low)
RI	1*	D In	Ring Indicator control input (active low)
SUSPEND	17*	D Out	This pin is logic high when the CP2104 is in the USB Suspend state.
$\overline{SUSPEND}$	15*	D Out	This pin is logic low when the CP2104 is in the USB Suspend state.
GPIO.3	11*	D I/O	User-configurable input or output.
GPIO.2	12*	D I/O	User-configurable input or output.
GPIO.1	13*	D I/O	User-configurable input or output.
GPIO.0	14*	D I/O	User-configurable input or output.
NC	10*		This pin should be left unconnected or tied to V_{IO}.

***Note:** Pins can be left unconnected when not used.

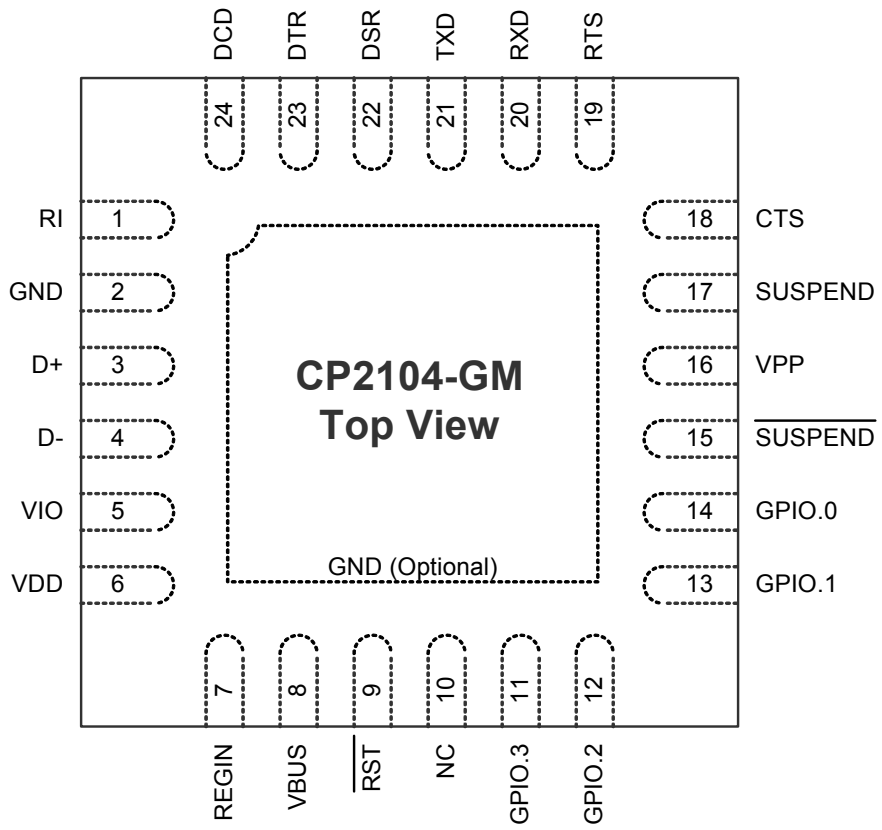


Figure 2. QFN-24 Pinout Diagram (Top View)

4. QFN-24 Package Specifications

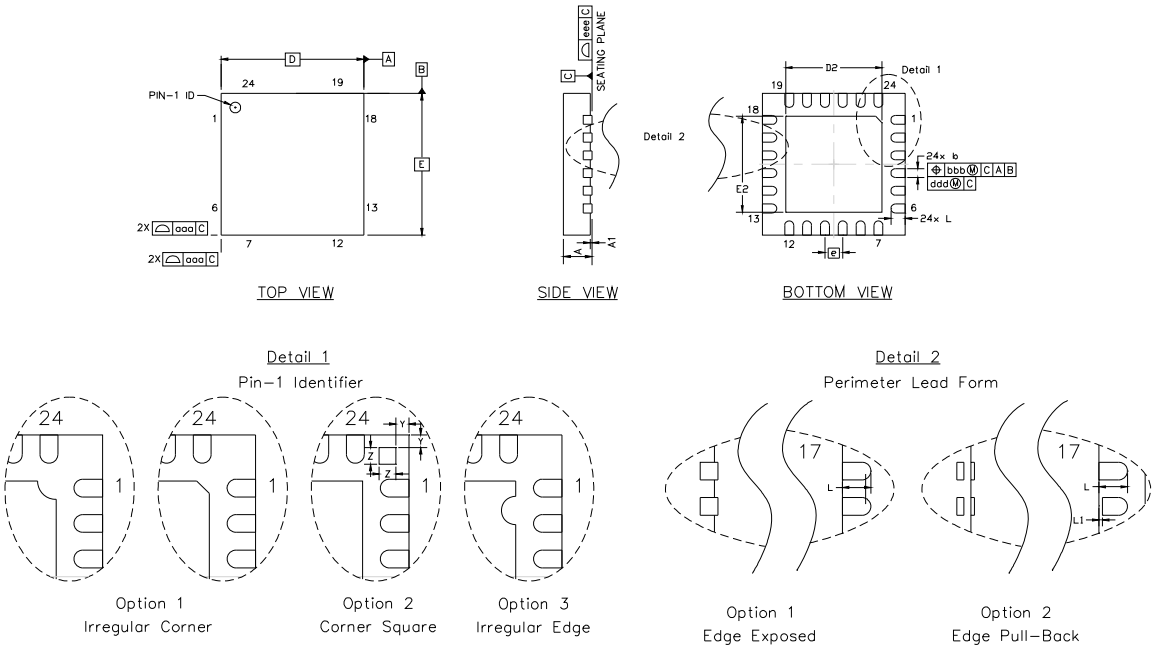


Figure 3. QFN-24 Package Drawing

Table 8. QFN-24 Package Dimensions

Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	0.70	0.75	0.80	L	0.30	0.40	0.50
A1	0.00	0.02	0.05	L1	0.00	—	0.15
b	0.18	0.25	0.30	aaa	—	—	0.15
D	4.00 BSC.			bbb	—	—	0.10
D2	2.55	2.70	2.80	ddd	—	—	0.05
e	0.50 BSC.			eee	—	—	0.08
E	4.00 BSC.			Z	—	0.24	—
E2	2.55	2.70	2.80	Y	—	0.18	—

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation WGGD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

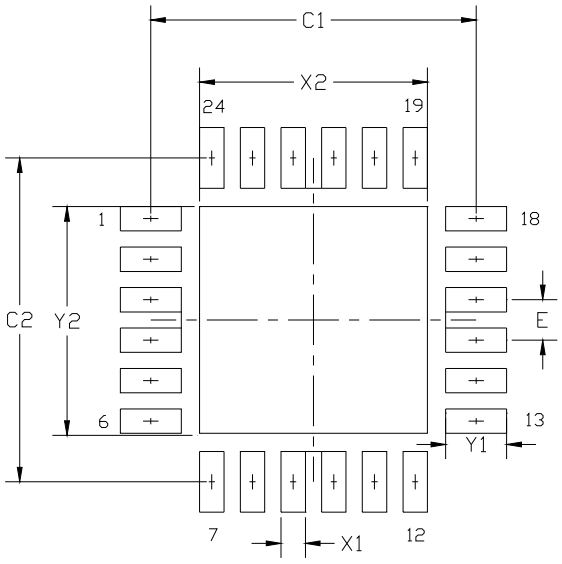


Figure 4. QFN-24 Recommended PCB Land Pattern

Table 9. QFN-24 PCB Land Pattern Dimensions

Dimension	Min	Max	Dimension	Min	Max
C1	3.90	4.00	X2	2.70	2.80
C2	3.90	4.00	Y1	0.65	0.75
E	0.50 BSC		Y2	2.70	2.80
X1	0.20	0.30			

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2x2 array of 1.10 mm x 1.10 mm openings on a 1.30 mm pitch should be used for the center pad.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5. USB Function Controller and Transceiver

The Universal Serial Bus (USB) function controller in the CP2104 is a USB 2.0 compliant full-speed device with integrated transceiver and on-chip matching and pullup resistors. The USB function controller manages all data transfers between the USB and the UART as well as command requests generated by the USB host controller and commands for controlling the function of the UART and GPIO pins.

The USB Suspend and Resume signals are supported for power management of both the CP2104 device as well as external circuitry. The CP2104 will enter Suspend mode when Suspend signaling is detected on the bus. On entering Suspend mode, the CP2104 asserts the SUSPEND and $\overline{\text{SUSPEND}}$ signals. SUSPEND and $\overline{\text{SUSPEND}}$ are also asserted after a CP2104 reset until device configuration during USB Enumeration is complete.

The CP2104 exits the Suspend mode when any of the following occur: Resume signaling is detected or generated, a USB Reset signal is detected, or a device reset occurs. On exit of Suspend mode, the SUSPEND and $\overline{\text{SUSPEND}}$ signals are de-asserted.

Both SUSPEND and $\overline{\text{SUSPEND}}$ temporarily float high during a CP2104 reset. If this behavior is undesirable, a strong pulldown (10 kΩ) can be used to ensure $\overline{\text{SUSPEND}}$ remains low during reset.

The logic level and output mode (push-pull or open-drain) of various pins during USB Suspend is configurable in the PROM. See Section 8 for more information.

6. Asynchronous Serial Data Bus (UART) Interface

The CP2104 UART interface consists of the TX (transmit) and RX (receive) data signals as well as the RTS, CTS, DSR, DTR, DCD, and RI control signals. The UART supports RTS/CTS, DSR/DTR, and X-On/X-Off handshaking.

The UART is programmable to support a variety of data formats and baud rates. If the Virtual COM Port drivers are used, the data format and baud rate are set during COM port configuration on the PC. If the USBXpress drivers are used, the CP2104 is configured through the USBXpress API. The data formats and baud rates available are listed in Table 10.

Table 10. Data Formats and Baud Rates

Data Bits[1]	5, 6, 7, and 8
Stop Bits	1, 1.5[2], and 2
Parity Type	None, Even, Odd, Mark, Space
Baud Rates	300 bps to 2.0 Mbps

Notes:
1. Data sizes of 5 and 6 bits are not supported at baud rates above 921600 bps.
2. 1.5 stop bits only available when using 5 data bits.

6.1. Baud Rate Generation

The baud rate generator is very flexible, allowing the user to request any baud rate in the range from 300 bps to 2 Mbps. If the baud rate cannot be directly generated from the 48 MHz oscillator, the device will choose the closest possible option. The actual baud rate is dictated by Equation 1 and Equation 2.

$$\text{Clock Divider} = \frac{48\ \text{MHz}}{2 \times \text{Prescale} \times \text{Requested Baud Rate}}$$

$$\text{Prescale} = 4 \text{ if Requested Baud Rate} \leq 365 \text{ bps}$$
$$\text{Prescale} = 1 \text{ if Requested Baud Rate} > 365 \text{ bps}$$

Equation 1. Clock Divider Calculation

$$\text{Actual Baud Rate} = \frac{48\ \text{MHz}}{2 \times \text{Prescale} \times \text{Clock Divider}}$$

$$\text{Prescale} = 4 \text{ if Requested Baud Rate} \leq 365 \text{ bps}$$
$$\text{Prescale} = 1 \text{ if Requested Baud Rate} > 365 \text{ bps}$$

Equation 2. Baud Rate Calculation

Most baud rates can be generated with an error of less than 1.0%. A general rule of thumb for the majority of UART applications is to limit the baud rate error on both the transmitter and the receiver to no more than ±2%. The clock divider value obtained in Equation 1 is rounded to the nearest integer, which may produce an error source. Another error source will be the 48 MHz oscillator, which is accurate to ±0.25%. Knowing the actual and requested baud rates, the total baud rate error can be found using Equation 3.

$$\text{Baud Rate Error (\%)} = 100 \times \left(1 - \frac{\text{Actual Baud Rate}}{\text{Requested Baud Rate}}\right) \pm 0.25\%$$

Equation 3. Baud Rate Error Calculation

7. GPIO Pins

The CP2104 supports four user-configurable GPIO pins for status and control information. Each of these GPIO pins are usable as inputs, open-drain outputs, or push-pull outputs. Three of these GPIO pins also have alternate functions which are listed in Table 11.

Table 11. GPIO Pin Alternate Functions

GPIO Pin	Alternate Function
GPIO.0	TX Toggle
GPIO.1	RX Toggle
GPIO.2	RS-485 Transceiver Control

By default, all of the GPIO pins are configured as a GPIO input. The configuration of the pins is one-time programmable for each device. The difference between an open-drain output and a push-pull output is when the GPIO output is driven to logic high. A logic high, open-drain output pulls the pin to the VIO rail through an internal, pull-up resistor. A logic high, push-pull output directly connects the pin to the VIO voltage. Open-drain outputs are typically used when interfacing to logic at a higher voltage than the VIO pin. These pins can be safely pulled to the higher, external voltage through an external pull-up resistor. The maximum external pull-up voltage is 5 V.

The speed of reading and writing the GPIO pins is subject to the timing of the USB bus. GPIO pins configured as inputs or outputs are not recommended for real-time signaling.

More information regarding the configuration and usage of these pins can be found in “AN721: CP21xx Device Customization Guide” and “AN223: Runtime GPIO Control for CP210x” available on the Silicon Labs website.

7.1. GPIO.0-1—Transmit and Receive Toggle

GPIO.0 and GPIO.1 are configurable as Transmit Toggle and Receive Toggle pins. These pins are logic high when a device is not transmitting or receiving data, and they toggle at a fixed rate as specified in Table 6 when data transfer is in progress. Typically, these pins are connected to two LEDs to indicate data transfer.

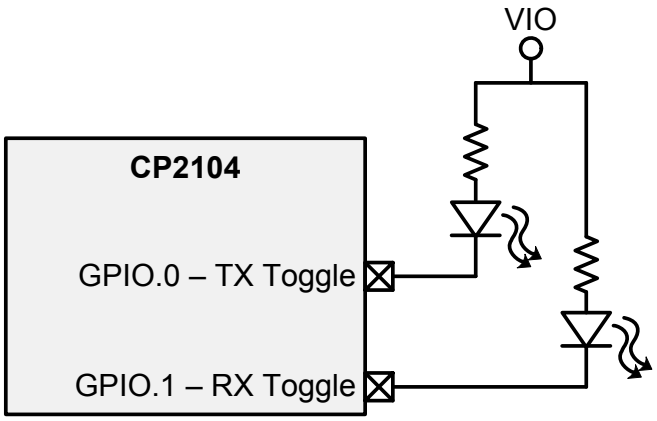


Figure 5. Transmit and Receive Toggle Typical Connection Diagram

7.2. GPIO.2—RS-485 Transceiver Bus Control

GPIO.2 is configurable as an RS-485 bus transceiver control pin which is connected to the DE and $\overline{RE}$ inputs of the transceiver. When configured for RS-485 mode, the pin is asserted during UART data transmission as well as line break transmission. The RS-485 mode of GPIO.2 is active-high by default, and is also configurable for active-low mode.

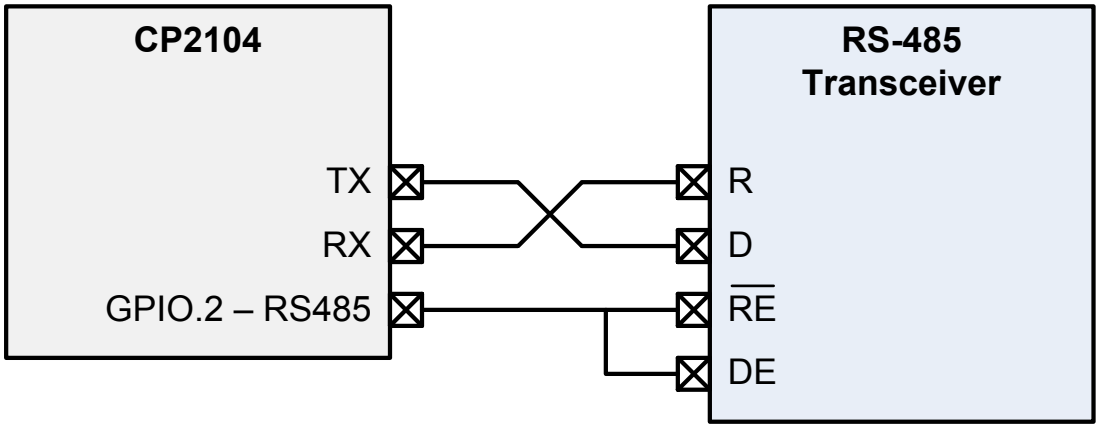


Figure 6. RS-485 Transceiver Typical Connection Diagram

7.3. Hardware Flow Control (RTS and CTS)

To utilize the functionality of the RTS and CTS pins of the CP2104, the device must be configured to use hardware flow control.

RTS, or Ready To Send, is an active-low output from the CP2104 and indicates to the external UART device that the CP2104's UART RX FIFO has not reached the watermark level of 383 bytes and is ready to accept more data. When the amount of data in the RX FIFO reaches the watermark, the CP2104 pulls RTS high to indicate to the external UART device to stop sending data.

CTS, or Clear To Send, is an active-low input to the CP2104 and is used by the external UART device to indicate to the CP2104 when the external UART device's RX FIFO is getting full. The CP2104 will not send more than two bytes of data once CTS is pulled high.

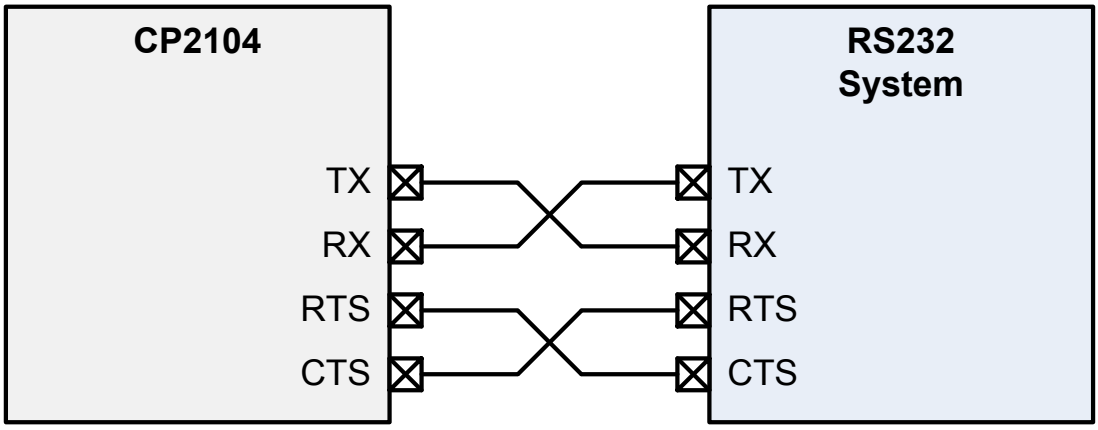


Figure 7. Hardware Flow Control Typical Connection Diagram

8. One-Time Programmable ROM

The CP2104 includes an internal one-time programmable ROM that may be used to customize the USB Vendor ID (VID), Product ID (PID), Product Description String, Power Descriptor, Device Release Number, Device Serial Number, GPIO configuration, Suspend pins, and modes as desired for OEM applications. If the programmable ROM has not been customized, the default configuration data shown in Table 12 and Table 13 is used.

Table 12. Default USB Configuration Data

Name	Value
Vendor ID	10C4h
Product ID	EA60h
Power Descriptor (Attributes)	80h (Bus-powered)
Power Descriptor (Max. Power)	32h (100 mA)
Release Number	0100h (Release Version 01.00)
Serial Number	Unique 8 character ASCII string (63 characters maximum)
Product Description String	“CP2104 USB to UART Bridge Controller” (126 characters maximum)

Table 13. Default GPIO, UART, and Suspend Configuration Data

Name	Value
GPIO.0	GPIO Input
GPIO.1	GPIO Input
GPIO.2	GPIO Input
GPIO.3	GPIO Input
Flush_Buffers	Flush TX and RX FIFO on open
SUSPEND	Push-pull
$\overline{\text{SUSPEND}}$	Push-pull
RS-485 Level	Active-High

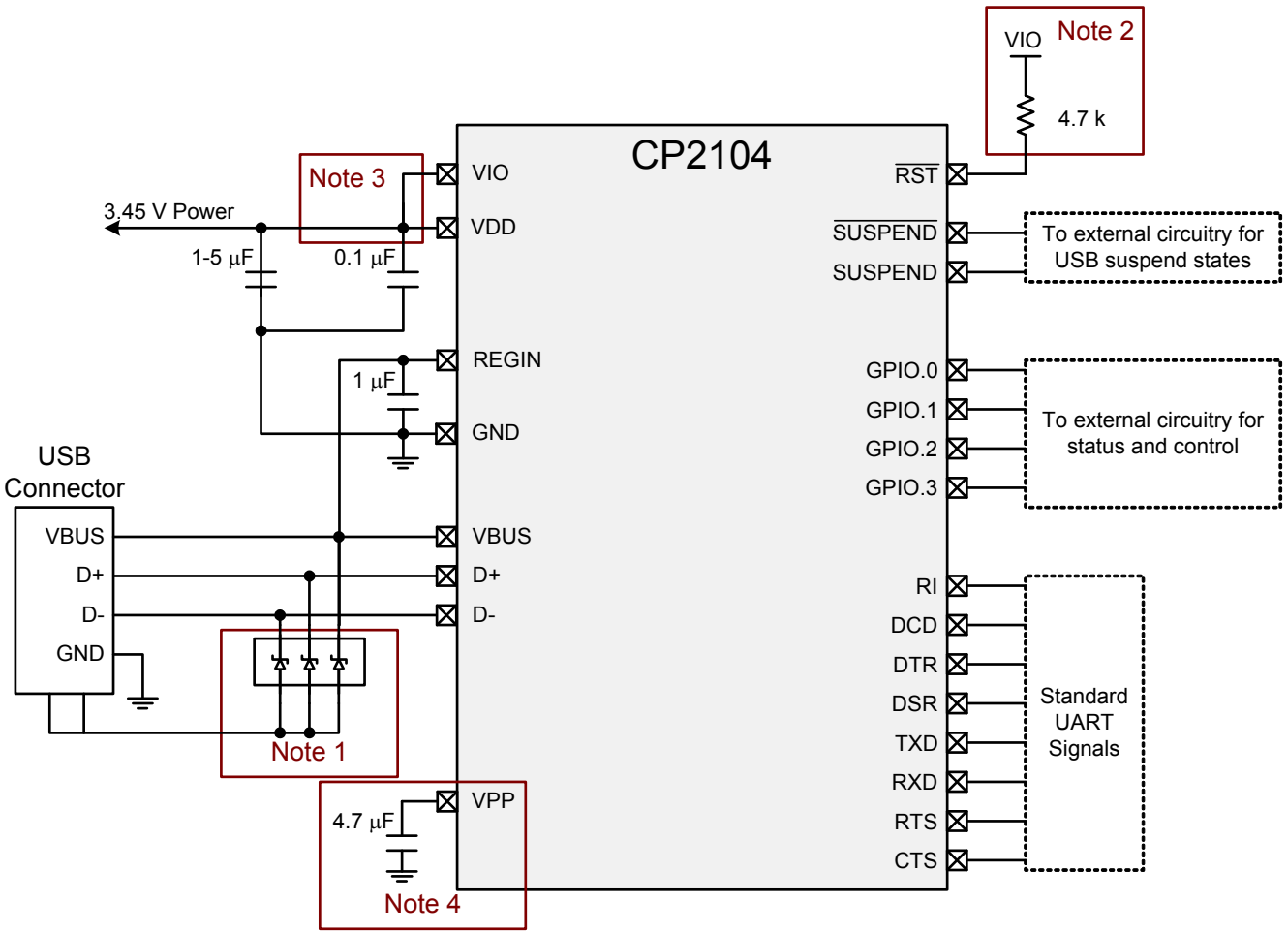
While customization of the USB configuration data is optional, customizing the VID/PID combination is recommended. A unique VID/PID combination will prevent the driver from conflicting with any other USB driver. A vendor ID can be obtained from www.usb.org or Silicon Labs can provide a free PID for the OEM product that can be used with the Silicon Labs VID. Customizing the serial number is also recommended if the OEM application is one in which it is possible for multiple CP210x-based devices to be connected to the same PC.

The configuration data ROM can be programmed by Silicon Labs prior to shipment with the desired configuration information. It can also be programmed in-system over the USB interface by adding a capacitor to the PCB. If configuration ROM is to be programmed in-system, a 4.7 µF capacitor must be added between the VPP pin and ground. No other circuitry should be connected to VPP during a programming operation, and V_{DD} must remain at 3.3 V or higher to successfully write to the configuration ROM.

9. Voltage Regulator

The CP2104 includes an on-chip 5.0 to 3.45 V voltage regulator. This allows the CP2104 to be configured as either a USB bus-powered device or a USB self-powered device. A typical connection diagram of the device in a bus-powered application using the regulator is shown in Figure 8. When enabled, the voltage regulator output appears on the V_{DD} pin and can be used to power external devices. See Table 5 for the voltage regulator electrical characteristics.

If the regulator is used to provide V_{DD} in a self-powered application, use the same connections from Figure 8, but connect REGIN to an onboard 5 V supply, and disconnect it from the VBUS pin. In addition, if REGIN may be unpowered while VBUS is 5 V, a resistor divider shown in Note 5 of Figure 9 is required to meet the absolute maximum voltage on VBUS specification in Table 1.

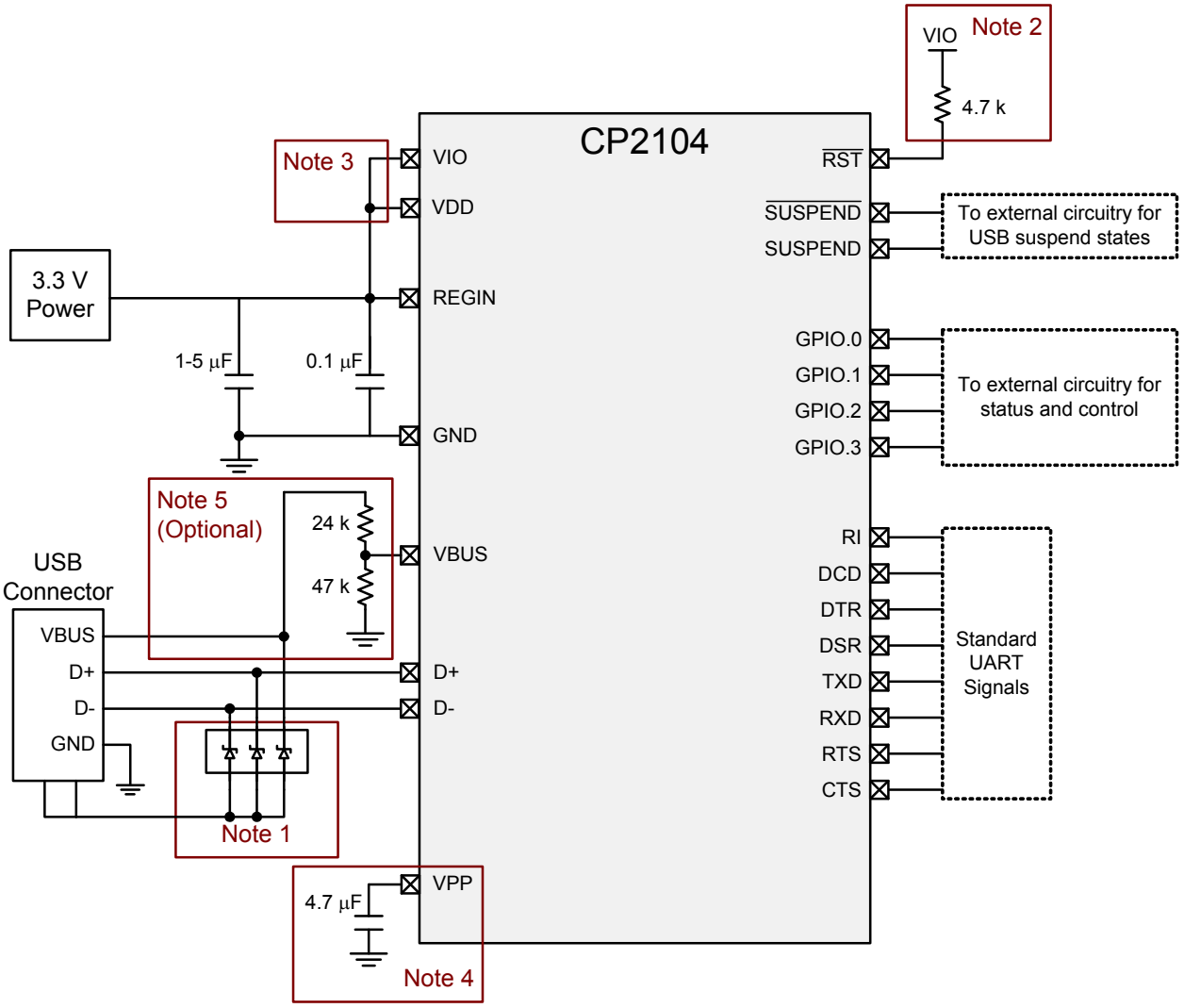


Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.
Note 2 : An external pull-up is not required, but can be added for noise immunity.
Note 3 : VIO can be connected directly to VDD or to a supply as low as 1.8 V to set the I/O interface voltage.
Note 4 : If configuration ROM is to be programmed via USB, a 4.7 µF capacitor must be added between VPP and ground. During a programming operation, the pin should not be connected to other circuitry, and VDD must be at least 3.3 V.

Figure 8. Typical Bus-Powered Connection Diagram

Alternatively, if 3.0 to 3.6 V power is supplied to the V_{DD} pin, the CP2104 can function as a USB self-powered device with the voltage regulator bypassed. For this configuration, tie the REGIN input to V_{DD} to bypass the voltage regulator. A typical connection diagram showing the device in a self-powered application with the regulator bypassed is shown in Figure 9.

The USB max power and power attributes descriptor must match the device power usage and configuration. See application note “AN721: CP210x/CP211x Device Customization Guide” for information on how to customize USB descriptors for the CP2104.



Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.
Note 2 : An external pull-up is not required, but can be added for noise immunity.
Note 3 : VIO can be connected directly to VDD or to a supply as low as 1.8 V to set the I/O interface voltage.
Note 4 : If configuration ROM is to be programmed via USB, a 4.7 µF capacitor must be added between VPP and ground. During a programming operation, the pin should not be connected to other circuitry, and VDD must be at least 3.3 V.
Note 5 : For self-powered systems where VDD and VIO may be unpowered when VBUS is connected to 5 V, a resistor divider (or functionally-equivalent circuit) on VBUS is required to meet the absolute maximum voltage on VBUS specification in the Electrical Characteristics section.

Figure 9. Typical Self-Powered Connection Diagram (Regulator Bypass)

10. CP2104 Device Drivers

There are two sets of device drivers available for CP2104 devices: the Virtual COM Port (VCP) drivers and the USBXpress Direct Access drivers. Only one set of drivers is necessary to interface with the device.

The latest drivers are available at http://www.siliconlabs.com/products/mcu/Pages/SoftwareDownloads.aspx.

10.1. Virtual COM Port Drivers

The CP2104 Virtual COM Port (VCP) device drivers allow a CP2104-based device to appear to the PC's application software as a COM port. Application software running on the PC accesses the CP2104-based device as it would access a standard hardware COM port. However, actual data transfer between the PC and the CP2104 device is performed over the USB interface. Therefore, existing COM port applications may be used to transfer data via the USB to the CP2104-based device without modifying the application. See application note “AN197: Serial Communications Guide for the CP210x” for Example Code for Interfacing to a CP2104 using the Virtual COM drivers.

10.2. USBXpress Drivers

The Silicon Labs USBXpress drivers provide an alternate solution for interfacing with CP2104 devices. No serial port protocol expertise is required. Instead, a simple, high-level application program interface (API) is used to provide simpler CP210x connectivity and functionality. The USBXpress for CP210x Development Kit includes Windows device drivers, Windows device driver installer and uninstallers, and a host interface function library (host API) provided in the form of a Windows dynamic link library (DLL). The USBXpress driver set is recommended for new products that also include new PC software. The USBXpress interface is described in application note “AN169: USBXpress Programmer's Guide.”

10.3. Driver Customization

In addition to customizing the device as described in "6. Asynchronous Serial Data Bus (UART) Interface" on page 12, the drivers and the drivers installation package can be also be customized. See application note “AN220: USB Driver Customization” for more information on generating customized VCP and USBXpress drivers.

Important Note: The VID/PID in the drivers must match the VID/PID in the device for the drivers to load properly then the device is connected to the PC.

10.4. Driver Certification

The default drivers that are shipped with the CP2104 are Microsoft Windows Hardware Quality Labs (WHQL) certified. The certification means that the drivers have been tested by Microsoft and their latest operating systems will allow the drivers to be installed without any warnings or errors.

The customized drivers that are generated using the “AN220: USB Driver Customization” software are not automatically certified. To become certified, they must go first through the Microsoft Driver Reseller Submission process. Contact Silicon Labs support for assistance with this process.

11. Relevant Application Notes

The following Application Notes are applicable to the CP2104. The latest versions of these application notes and their accompanying software are available at http://www.siliconlabs.com/products/mcu/Pages/ApplicationNotes.aspx.

- AN721: CP21xx Device Customization Guide—This application note describes how to use the AN721 software CP21xxCustomizationUtility to configure the USB parameters on the CP21xx devices.
- AN169: USBXpress Programmer's Guide—This application note describes the USBXpress API interface and includes example code.
- AN197: Serial Communications Guide for the CP210x—This application note describes how to use the standard Windows COM port function to communicate with the CP210x and includes example code.
- AN220: USB Driver Customization—This application note describes how to use the AN220 software to customize the VCP or USBXpress drivers with OEM information.
- AN223: Runtime GPIO Control for CP210x—This application note describes how to use the CP210xRuntime DLL to control the CP210x GPIO.

Document Change List

Revision 0.2 to Revision 0.3

- Updated Figure 1, “Example System Diagram,” on page 1.
- Added Figure , “,” on page 11.
- Added Figure 8, “Typical Bus-Powered Connection Diagram,” on page 17.
- Added Figure 9, “Typical Self-Powered Connection Diagram (Regulator Bypass),” on page 18.
- Added "6.1. Baud Rate Generation" on page 13.
- Moved Table 5 to "2. Electrical Characteristics" on page 5.

Revision 0.3 to Revision 0.4

- Updated ordering part number on page 1.
- Updated self-powered supply voltage on page 1.
- Updated USB pull-up supply current in table 2.
- Updated output voltage in Table 5.
- Updated Table 7 pin descriptions.
- Updated Table 10 baud rates.
- Updated Figure 9.

Revision 0.4 to Revision 1.0

- Updated ordering part number on page 1.
- Updated electrical specifications throughout Section 2.
- Added Table 6
- Updated Section 7.
- Updated Section 8.
- Added Table 11 and Table 13
- Updated descriptions of figures in Section 9.

Revision 1.0 to Revision 1.1

- Added a row for VBUS in Table 1, “Absolute Maximum Ratings,” on page 5.
- Added V_{DD} Ramp Time for Power On specification to Table 4, “Reset Electrical Characteristics,” on page 6.
- Added V_{PP} Voltage and Capacitor specifications to Table 2, “Global DC Electrical Characteristics,” on page 5.
- Updated AN144 references to AN721.
- Updated "9. Voltage Regulator" on page 17 to add absolute maximum voltage on VBUS requirements in self-powered systems.

Revision 1.1 to Revision 1.2

January 20, 2017

- Added note on front page.