CP2105

SINGLE-CHIP USB TO DUAL UART BRIDGE

Single-Chip USB to Dual UART Data Transfer
- Integrated USB transceiver; no external resistors required
- Integrated clock; no external crystal required
- Integrated 296-Byte One-Time Programmable ROM for storing customizable product information
- On-chip power-on reset circuit
- On-chip voltage regulator: 3.45 V output

USB Peripheral Function Controller
- USB Specification 2.0 compliant; full-speed (12 Mbps)
- USB Suspend states supported via SUSPEND pins

Two UART Interfaces ("Enhanced" and "Standard")
- Flow control options:
  - Hardware (CTS / RTS)
  - Software (X-On / X-Off)
  - No flow control
- Configurable I/O (1.8 V to V_{DD}) using V_{IO} pin
- Configurable I/O (V_{DD} to 5 V) using external pull-up
- All modem interface signals available (when GPIO is not used)

Enhanced UART Interface Features
- Data formats supported:
  - Data bits: 5, 6, 7, and 8
  - Stop bits: 1, 1.5, and 2
  - Parity: odd, even, mark, space, no parity
- Baud rates: 300 bps to 2.0 Mbps
- 320 Byte receive and transmit buffers
- Two GPIO signals for status and control
- RS-485 mode with bus transceiver control

Standard UART Interface Features
- Data format: 8 data bits, 1 Stop bit
- Parity: Even, Odd, No parity
- Baud rates: 2400 bps to 921600 bps
- 288 Byte receive and transmit buffers
- Three GPIO signals for status and control

Virtual COM Port Device Drivers
- Works with Existing COM Port PC Applications
- Royalty-Free Distribution License
- Windows 7/Vista/XP/Server 2003/2000
- Mac OS-X
- Linux

USBXpress™ Direct Driver Support
- Royalty-Free Distribution License
- Windows 7/Vista/XP/Server 2003/2000
- Windows CE 6.0, 5.0, and 4.2

Supply Voltage
- Self-powered: 3.0 to 3.6 V
- USB bus powered: 4.0 to 5.25 V
- I/O voltage: 1.8 V to V_{DD}

Package
- RoHS-compliant 24-pin QFN (4 x 4 mm)

Ordering Part Number
- CP2105-F01-GM

Temperature Range: –40 to +85 °C

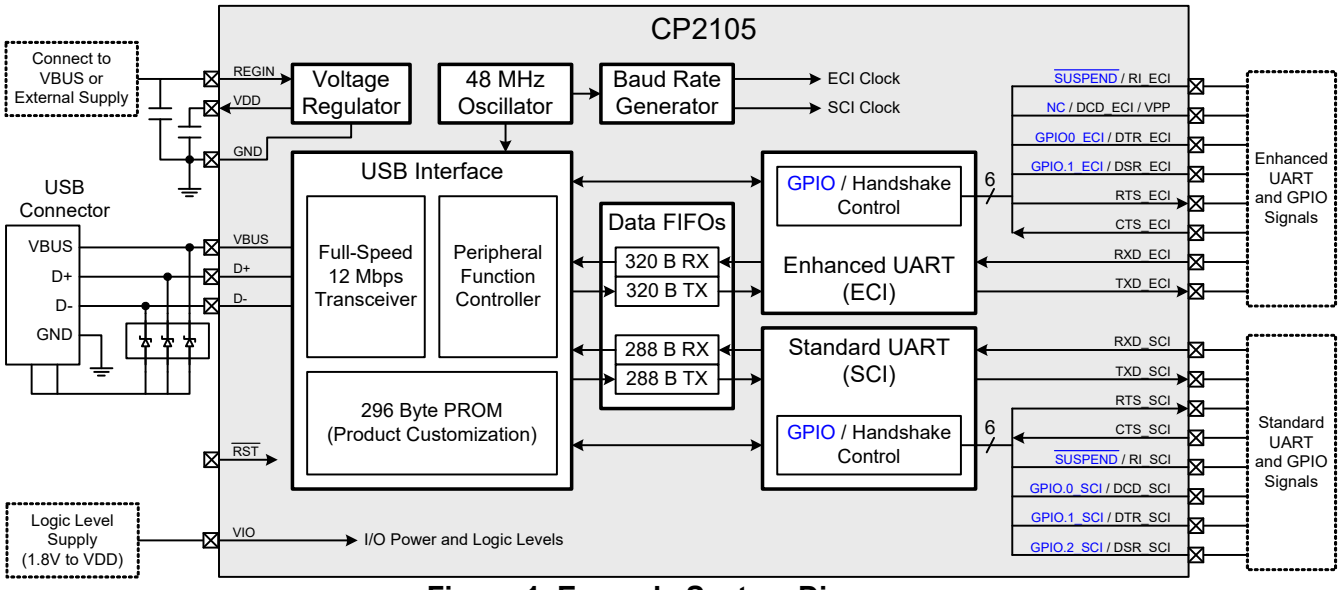


Figure 1. Example System Diagram

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1. System Overview

The CP2105 is a highly integrated USB-to-Dual-UART Bridge Controller providing a simple solution for updating RS-232 designs to USB using a minimum of components and PCB space. The CP2105 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, one-time programmable ROM, and two asynchronous serial data buses (UART) with full modem control signals in a compact 4 x 4 mm QFN-24 package (sometimes called “MLF” or “MLP”).

The on-chip one-time programmable ROM may be used to customize the USB Vendor ID, Product ID, Product Description String, Power Descriptor, Device Release Number, Interface Strings, Device Serial Number, and Modem/GPIO configuration as desired for OEM applications.

Royalty-free Virtual COM Port (VCP) device drivers provided by Silicon Labs allow a CP2105-based product to appear as two COM ports in PC applications. The CP2105 UART interfaces implement all RS-232 signals including control and handshaking, so existing system firmware does not need to be modified. The device also features a total of five GPIO signals that can be user-defined for status and control information. Support for I/O interface voltages down to 1.8 V is provided via a V_{IO} pin. Direct access driver support is also available through the Silicon Labs USBXpress driver set. See www.silabs.com for the latest application notes and product support information for the CP2105.

An evaluation kit for the CP2105 (Part Number: CP2105EK) is available. It includes a CP2105-based USB-to-UART/RS-232 evaluation board, a complete set of VCP device drivers, USB and RS-232 cables, and full documentation. Contact a Silicon Labs sales representatives or go to www.silabs.com to order the CP2105 Evaluation Kit.

2. Electrical Characteristics

Table 1. Absolute Maximum Ratings

Parameter	Test Condition	Min	Typ	Max	Unit
Ambient Temperature Under Bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on $\overline{RST}$, GPIO or UART Pins with respect to GND	$V_{IO} \geq 2.2$ V $V_{IO} < 2.2$ V	–0.3 –0.3	— —	5.8 V_{IO} + 3.6	V
Voltage on VBUS with respect to GND	$V_{DD} \geq 3.0$ V V_{DD} not powered	–0.3 –0.3	— —	5.8 V_{DD} + 3.6	V
Voltage on V_{DD} or V_{IO} with respect to GND		–0.3	—	4.2	V
Maximum Total Current through V_{DD}, V_{IO}, and GND		—	—	500	mA
Maximum Output Current Sunk by $\overline{RST}$ or any I/O pin		—	—	100	mA

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at or exceeding the conditions in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Global DC Electrical Characteristics

V_{DD} = 3.0 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
Digital Supply Voltage (V_{DD})		3.0	—	3.6	V
Digital Port I/O Supply Voltage (V_{IO})		1.8	—	V_{DD}	V
Voltage on V_{PP} with respect to GND during a ROM programming operation	$V_{IO} \geq 3.3$ V	5.75	—	V_{IO} + 3.6	V
Capacitor on V_{PP} for ROM programming		—	4.7	—	µF
Supply Current[1]	Normal Operation; V_{REG} Enabled	—	17	18.5	mA
Supply Current[1]	Suspended; V_{REG} Enabled	—	100	220	µA
Supply Current - USB Pull-up[2]		—	200	228	µA
Specified Operating Temperature Range		–40	—	+85	°C

Notes:
1. If the device is connected to the USB bus, the USB Pull-up Current should be added to the supply current for total supply current.
2. The USB Pull-up supply current values are calculated values based on USB specifications.

Table 3. UART and Suspend I/O DC Electrical Characteristics

V_{DD} = 3.0 to 3.6 V, V_{IO} = 1.8 V to V_{DD}, –40 to +85 °C unless otherwise specified.

Parameters	Test Condition	Min	Typ	Max	Unit
Output High Voltage (V_{OH})	I_{OH} = –10 µA I_{OH} = –3 mA I_{OH} = –10 mA	V_{IO} – 0.1 V_{IO} – 0.2 —	— — V_{IO} – 0.4	— — —	V
Output Low Voltage (V_{OL})	I_{OL} = 10 µA I_{OL} = 8.5 mA I_{OL} = 25 mA	— — —	— — 0.6	0.1 0.4 —	V
Input High Voltage (V_{IH})		0.7 x V_{IO}	—	—	V
Input Low Voltage (V_{IL})		—	—	0.6	V
Input Leakage Current	Weak Pull-Up Off Weak Pull-Up On, V_{IO} = 0 V	— —	— 25	1 50	µA
Maximum Input Voltage	Open drain, logic high (1)	—	—	5.8	V

Table 4. Reset Electrical Characteristics

–40 to +85 °C unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
$\overline{RST}$ Input High Voltage		0.75 x V_{IO}	—	—	V
$\overline{RST}$ Input Low Voltage		—	—	0.6	V
Minimum $\overline{RST}$ Low Time to Generate a System Reset		15	—	—	µs
V_{DD} Ramp Time for Power On		—	—	1	ms

Table 5. Voltage Regulator Electrical Specifications

–40 to +85 °C unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Units
Input Voltage Range		3.0	—	5.25	V
Output Voltage	Output Current = 1 to 100 mA*	3.3	3.45	3.6	V
VBUS Detection Input Threshold		2.5	—	—	V
Bias Current		—	—	120	µA
***Note:** The maximum regulator supply current is 100 mA. This includes the supply current of the CP2105.					

Table 6. GPIO Output Specifications

–40 to +85 °C unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
RS-485 Active Time After Stop Bit		—	1	—	bit time*
TX Toggle Rate		—	7.5	—	Hz
RX Toggle Rate		—	7.5	—	Hz
***Note:** Bit-time is calculated as 1 / baud rate.					

3. Pinout and Package Definitions

Table 7. CP2105 Pin Definitions

Name	Pin #	Type	Description
V_{DD}	6	Power In	Power Supply Voltage Input.
		Power Out	Voltage Regulator Output. See Section 10.
V_{IO}	5	Power In	I/O Supply Voltage Input.
GND	2		Ground. Must be tied to ground.
$\overline{RST}$	9	D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for the time specified in Table 4.
REGIN	7	Power In	5 V Regulator Input. This pin is the input to the on-chip voltage regulator.
VBUS	8	D In	VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network.
D+	3	D I/O	USB D+
D–	4	D I/O	USB D–
$\overline{SUSPEND}$	1*	D Out	In GPIO mode, this pin indicates whether the device is in the USB Suspend or not. The polarity can be configured via the configuration PROM, and defaults to active-low.
RI_SCI		D In	In modem control mode, this pin is the Ring Indicator control input (active low) for the Standard Comm Interface.
GPIO.0_SCI	24*	D I/O	In GPIO mode, this pin is a user-configurable input or output for the Standard Comm Interface.
DCD_SCI		D In	In modem control mode, this pin is the Data Carrier Detect control input (active low) for the Standard Comm Interface.
GPIO.1_SCI	23*	D I/O	In GPIO mode, this pin is a user-configurable input or output for the Standard Comm Interface.
DTR_SCI		D Out	In modem control mode, this pin is the Data Terminal Ready control output (active low) for the Standard Comm Interface.
GPIO.2_SCI	22*	D I/O	In GPIO mode, this pin is a user-configurable input or output for the Standard Comm Interface.
DSR_SCI		D in	In modem control mode, this pin is the Data Set Ready control input (active low) for the Standard Comm Interface.
TXD_SCI	21	D Out	Asynchronous data output (UART Transmit) for the Standard Comm Interface.
RXD_SCI	20	D In	Asynchronous data input (UART Receive) for the Standard Comm Interface.
RTS_SCI	19*	D Out	Ready to Send control output (active low) for the Standard Comm Interface.

***Note:** Pins can be left unconnected when not used.

Table 7. CP2105 Pin Definitions (Continued)

Name	Pin #	Type	Description
CTS_SCI	18*	D In	Clear To Send control input (active low) for the Standard Comm Interface.
$\overline{\text{SUSPEND}}$	17*	D Out	In GPIO mode, this pin indicates whether the device is in the USB Suspend or not. The polarity can be configured via the configuration PROM, and defaults to active-low.
RI_ECI		D In	In modem control mode, this pin is the Ring Indicator control input (active low) for the Standard Comm Interface.
NC	16*	—	In GPIO mode, this pin is not used.
DCD_ECI		D In	In modem control mode, this pin is the Data Carrier Detect control input (active low) for the Enhanced Comm Interface.
V_{PP}		Special	Additionally, in either mode programming of the configuration ROM via the USB interface can be accomplished if a 4.7 µF capacitor is connected between this pin and GND.
GPIO.0_ECI	15*	D I/O	In GPIO mode, this pin is a user-configurable input or output for the Enhanced Comm Interface.
DTR_ECI		D Out	In modem control mode, this pin is the Data Terminal Ready control output (active low) for the Enhanced Comm Interface.
GPIO.1_ECI	14*	D I/O	In GPIO mode, this pin is a user-configurable input or output for the Enhanced Comm Interface.
DSR_ECI		D in	In modem control mode, this pin is the Data Set Ready control input (active low) for the Enhanced Comm Interface.
TXD_ECI	13	D Out	Asynchronous data output (UART Transmit) for the Enhanced Comm Interface.
RXD_ECI	12	D In	Asynchronous data input (UART Receive) for the Enhanced Comm Interface.
RTS_ECI	11*	D Out	Ready to Send control output (active low) for the Enhanced Comm Interface.
CTS_ECI	10*	D In	Clear To Send control input (active low) for the Enhanced Comm Interface.

***Note:** Pins can be left unconnected when not used.

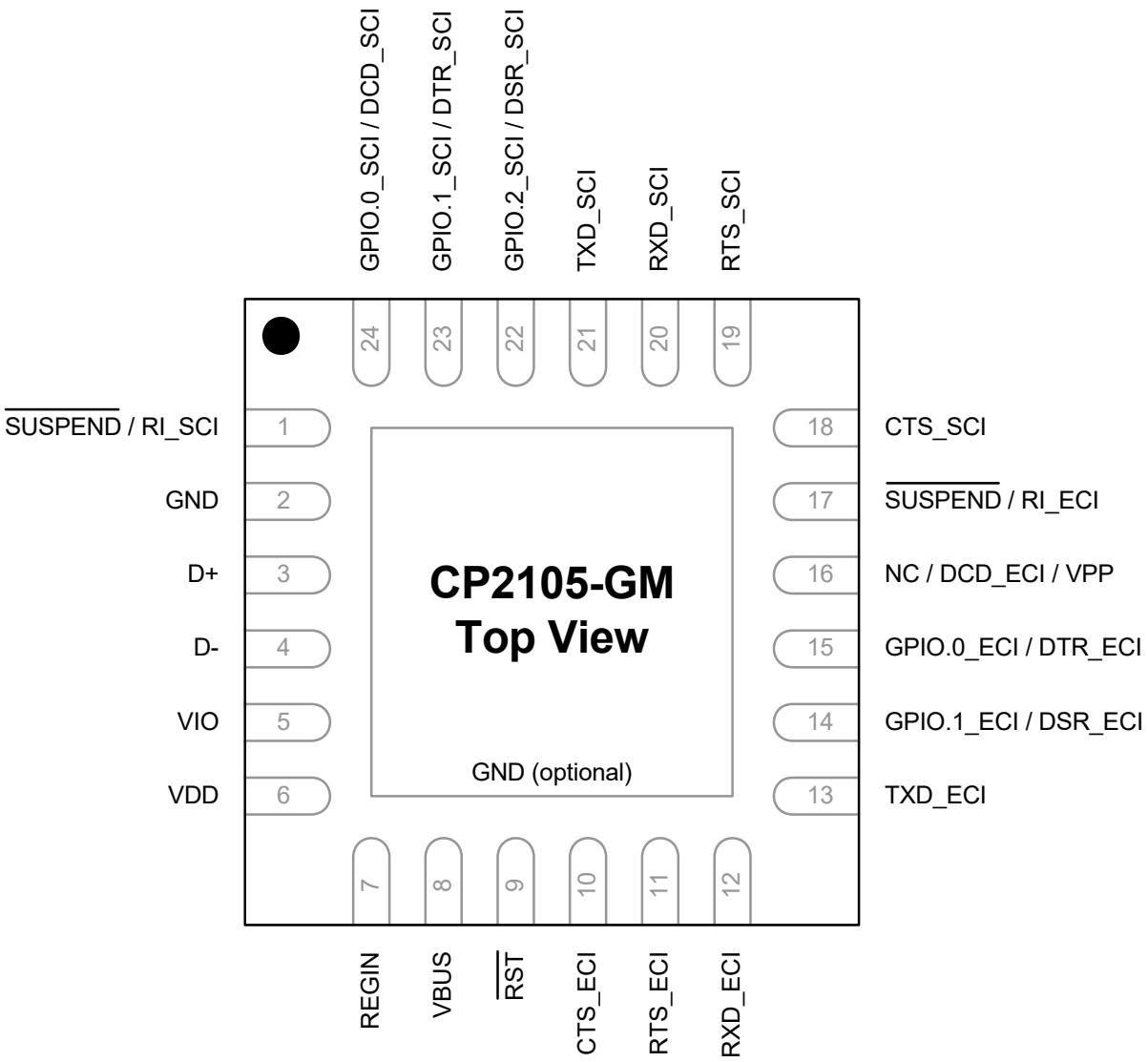


Figure 2. QFN-24 Pinout Diagram (Top View)

4. QFN-24 Package Specifications

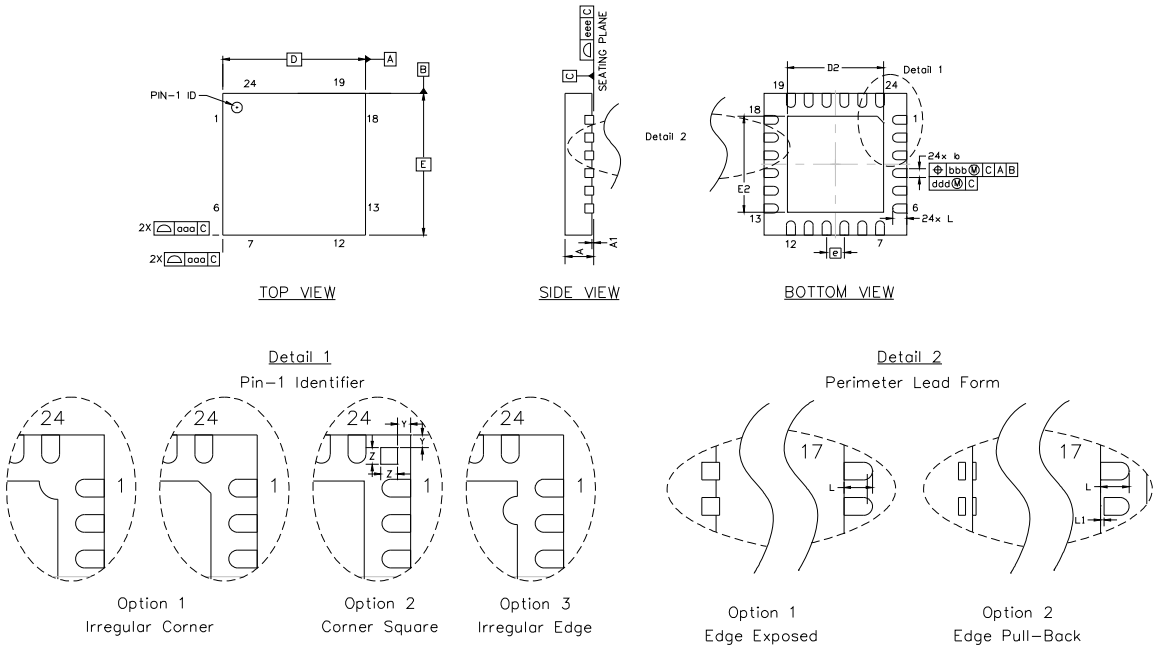


Figure 3. QFN-24 Package Drawing

Table 8. QFN-24 Package Dimensions

Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	0.70	0.75	0.80	L	0.30	0.40	0.50
A1	0.00	0.02	0.05	L1	0.00	—	0.15
b	0.18	0.25	0.30	aaa	—	—	0.15
D	4.00 BSC.			bbb	—	—	0.10
D2	2.55	2.70	2.80	ddd	—	—	0.05
e	0.50 BSC.			eee	—	—	0.08
E	4.00 BSC.			Z	—	0.24	—
E2	2.55	2.70	2.80	Y	—	0.18	—

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation WGGD except for custom features D2, E2, Z, Y, and L, which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

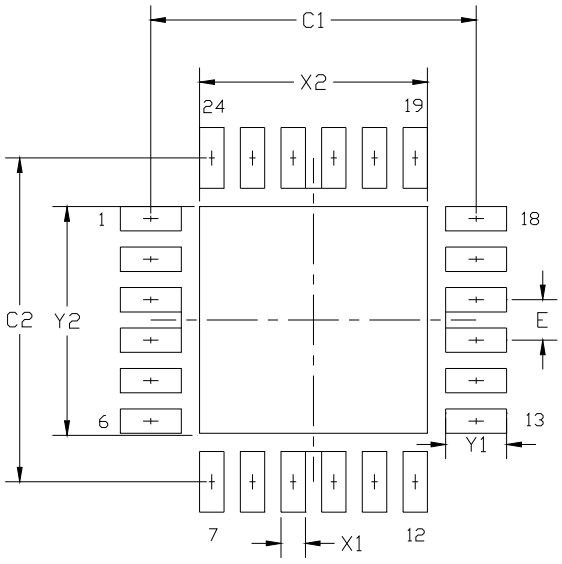


Figure 4. QFN-24 Recommended PCB Land Pattern

Table 9. QFN-24 PCB Land Pattern Dimensions

Dimension	Min	Max	Dimension	Min	Max
C1	3.90	4.00	X2	2.70	2.80
C2	3.90	4.00	Y1	0.65	0.75
E	0.50 BSC		Y2	2.70	2.80
X1	0.20	0.30			

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2x2 array of 1.10 x 1.10 mm openings on a 1.30 mm pitch should be used for the center pad.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5. USB Function Controller and Transceiver

The Universal Serial Bus (USB) function controller in the CP2105 is a USB 2.0 compliant full-speed device with integrated transceiver and on-chip matching and pullup resistors. The USB function controller manages all data transfers between the USB and the UARTs as well as command requests generated by the USB host controller and commands for controlling the function of the UARTs and GPIO pins.

The USB Suspend and Resume states are supported for power management of both the CP2105 device as well as external circuitry. The CP2105 will enter Suspend mode when Suspend signaling is detected on the bus. On entering Suspend mode, the SUSPEND signals will be asserted if the corresponding interface is configured for GPIO mode. SUSPEND is also asserted after a CP2105 reset until device configuration during USB Enumeration is complete. SUSPEND is active-low by default, but can be configured using the PROM to be active high.

The CP2105 exits the Suspend mode when any of the following occur: Resume signaling is detected or generated, a USB Reset signal is detected, or a device reset occurs. On exit of Suspend mode the SUSPEND signal is de-asserted. SUSPEND is weakly pulled to VIO in a high impedance state during a CP2105 reset. If this behavior is undesirable, a strong pulldown (10 kΩ) can be used to ensure SUSPEND remains low during reset.

The logic level and output mode (push-pull or open-drain) of various pins during USB Suspend is configurable in the PROM. See Section 9 for more information.

6. Asynchronous Serial Data Bus (UART) Interfaces

The CP2105 contains two UART interfaces, known as the Enhanced Communications Interface (ECI) and Standard Communications Interface (SCI)

Each UART interface consists of the TXD (transmit) and RXD (receive) data signals as well as RTS and CTS flow control signals. Optionally, the modem control signals DSR, DTR, DCD, and RI can be enabled for each interface. If modem control signals are not required for the application, these pins can be configured to operate with alternate functions, such as GPIO and SUSPEND signals. The UARTs support RTS/CTS, DSR/DTR, and X-On/X-Off handshaking. The UARTs are programmable to support a variety of data formats and baud rates. The ECI supports several additional UART configuration options beyond those supported by the SCI. If the Virtual COM Port drivers are used, the data format and baud rate are set during COM port configuration on the PC. If the USBXpress drivers are used, the CP2105 is configured through the USBXpress API. The data formats and baud rates available to each interface are listed in Table 10.

Table 10. Data Formats and Baud Rates

Interface	Enhanced Communication Interface (ECI)	Standard Communication Interface (SCI)
Data Bits[1]	5, 6, 7, and 8	8
Stop Bits	1, 1.5[2], and 2	1
Parity Type	None, Even, Odd, Mark, Space	None, Even, Odd
Baud Rate	300 bps to 2.0 Mbps[3]	2400, 4800, 7200, 9600, 14400, 19200, 28800, 38400, 56000, 57600, 115200, 128000, 230400, 460800, 921600

Notes:
1. Data sizes of 5 and 6 bits are not supported at baud rates above 921600 bps.
2. 1.5 stop bits only available when using 5 data bits.
3. See “6.1. ECI Baud Rate Generation” for more details on possible baud rates for the ECI interface.

6.1. ECI Baud Rate Generation

The baud rate generator for the enhanced interface is very flexible, allowing the user to request any baud rate in the range from 300 bps to 2.0 Mbps. If the baud rate cannot be directly generated from the 48 MHz oscillator, the device will choose the closest possible option. The actual baud rate is dictated by Equation 1 and Equation 2.

$$\text{Clock Divider} = \frac{48\ \text{MHz}}{2 \times \text{Prescale} \times \text{Requested Baud Rate}}$$

$$\text{Prescale} = 4 \text{ if Requested Baud Rate} \leq 365 \text{ bps}$$
$$\text{Prescale} = 1 \text{ if Requested Baud Rate} > 365 \text{ bps}$$

Equation 1. Clock Divider Calculation

$$\text{Actual Baud Rate} = \frac{48\ \text{MHz}}{2 \times \text{Prescale} \times \text{Clock Divider}}$$

$$\text{Prescale} = 4 \text{ if Requested Baud Rate} \leq 365 \text{ bps}$$
$$\text{Prescale} = 1 \text{ if Requested Baud Rate} > 365 \text{ bps}$$

Equation 2. Baud Rate Calculation

Most baud rates can be generated with an error of less than 1.0%. A general rule of thumb for the majority of UART applications is to limit the baud rate error on both the transmitter and the receiver to no more than ±2%. The clock divider value obtained in Equation 1 is rounded to the nearest integer, which may produce an error source. Another error source will be the 48 MHz oscillator, which is accurate to ±0.25%. Knowing the actual and requested baud rates, the total baud rate error can be found using Equation 3.

$$\text{Baud Rate Error (\%)} = 100 \times \left(1 - \frac{\text{Actual Baud Rate}}{\text{Requested Baud Rate}}\right) \pm 0.25\%$$

Equation 3. Baud Rate Error Calculation

The UART also supports the transmission of a line break. It can be set to transmit indefinitely until a stop command is sent from the application.

7. GPIO Mode and Modem Mode

Each interface on the CP2105 can be configured in either GPIO Mode or Modem Mode. This allows the SCI and ECI to have either modem control signals or GPIO signals available at various pins. Table 11 shows the functions that are available in each mode.By default, both interfaces are configured for GPIO Mode.

Table 11. CP2105 Modem Mode and GPIO Mode

Interface	Pin #	Modem Mode	GPIO Mode
Standard Communications Interface	24	DCD_SCI	GPIO_0_SCI
	23	DTR_SCI	GPIO_1_SCI
	22	DSR_SCI	GPIO_2_SCI
	1	RI_SCI	$\overline{\text{SUSPEND}}$_SCI
Enhanced Communications Interface	15	DTR_ECI	GPIO_0_ECI
	14	DSR_ECI	GPIO_1_ECI
	17	RI_ECI	$\overline{\text{SUSPEND}}$_ECI

Only one mode can be selected for each interface. Also, the mode of the CP2105 can only be configured once and cannot be reset to the default configuration after being programmed. Refer to “AN223: Runtime GPIO Control for CP210x” for more information on how to configure the port pins of the CP2105.

8. GPIO Pins

The CP2105 supports five user-configurable GPIO pins for status and control information. The Standard Communication Interface (SCI) has three GPIO pins and the Enhanced Communication Interface (ECI) has two GPIO pins. To use the pins as GPIO pins, the interface with the GPIO pins must be configured in GPIO Mode. By default, both communication interfaces on the CP2105 are configured for GPIO Mode. If the Modem Control signals are needed, the interface must be configured for Modem Mode. See Section 7 for more information on Modem Mode.

Each of these GPIO pins are usable as inputs, open-drain outputs, or push-pull outputs. Four of the GPIO pins also have alternate functions listed in Table 12 (GPIO.2_SCI does not have an alternate function).

Table 12. GPIO Mode Alternate Functions

GPIO Pin	Alternate Function
GPIO.0_ECI	TX Toggle
GPIO.1_ECI	RX Toggle/RS-485 Transceiver Control
GPIO.0_SCI	TX Toggle
GPIO.1_SCI	RX Toggle

By default, all of the GPIO pins are configured as a GPIO input. The configuration of the pins is one-time programmable for each device. The difference between an open-drain output and a push-pull output is when the GPIO output is driven to logic high. A logic high, open-drain output pulls the pin to the VIO rail through an internal, pull-up resistor. A logic high, push-pull output directly connects the pin to the VIO voltage. Open-drain outputs are typically used when interfacing to logic at a higher voltage than the VIO pin. These pins can be safely pulled to the higher, external voltage through an external pull-up resistor. The maximum external pull-up voltage is 5 V.

The speed of reading and writing the GPIO pins is subject to the timing of the USB bus. GPIO pins configured as inputs or outputs are not recommended for real-time signalling.

More information regarding the configuration and usage of these pins can be found in “AN721: CP21xx Device Customization Guide” and “AN223: Runtime GPIO Control for CP210x” available on the Silicon Labs website.

8.1. GPIO.0-1—Transmit and Receive Toggle

GPIO.0 and GPIO.1 are configurable as Transmit Toggle and Receive Toggle pins for both the Enhanced Communication Interface and the Standard Communication Interface. These pins are logic high when a device is not transmitting or receiving data, and they toggle at a fixed rate as specified in Table 6 when data transfer is in progress. Typically, these pins are connected to two LEDs to indicate data transfer.

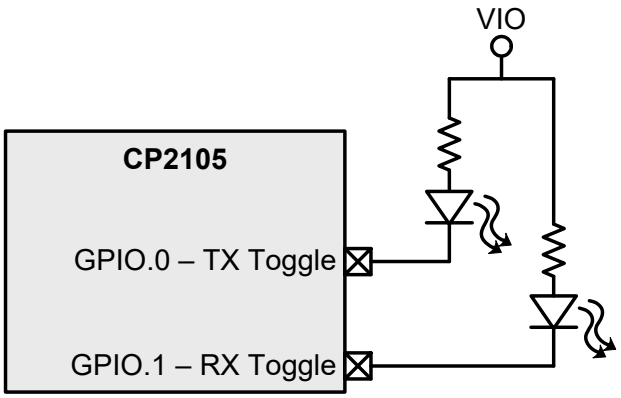


Figure 5. Transmit and Receive Toggle Typical Connection Diagram

8.2. GPIO.1_ECI—RS-485 Transceiver Bus Control

GPIO.1_ECI is configurable as an RS-485 bus transceiver control pin or the Enhanced Communication Interface which is connected to the DE and $\overline{RE}$ inputs of the transceiver. When configured for RS-485 mode, the pin is asserted during UART data transmission as well as line break transmission and the RX Toggle mode is not available. The RS-485 mode of GPIO.1_ECI is active-high by default, and is also configurable for active-low mode.

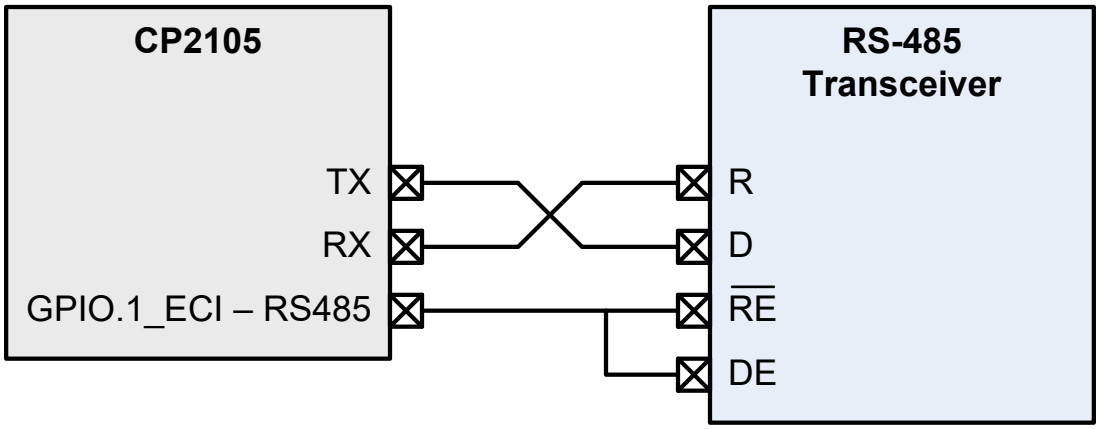


Figure 6. RS-485 Transceiver Typical Connection Diagram

8.3. Hardware Flow Control (RTS and CTS)

To utilize the functionality of the RTS and CTS pins of the CP2105, the device must be configured to use hardware flow control.

RTS, or Ready To Send, is an active-low output from the CP2105 and indicates to the external UART device that the CP2105's UART RX FIFO has not reached the watermark level of 191 bytes on the Enhanced Communication interface or 63 bytes on the Standard Communication Interface and is ready to accept more data. When the amount of data in the RX FIFO reaches the watermark, the CP2105 pulls RTS high to indicate to the external UART device to stop sending data.

CTS, or Clear To Send, is an active-low input to the CP2105 and is used by the external UART device to indicate to the CP2105 when the external UART device's RX FIFO is getting full. The CP2105 will not send more than two bytes of data once CTS is pulled high.

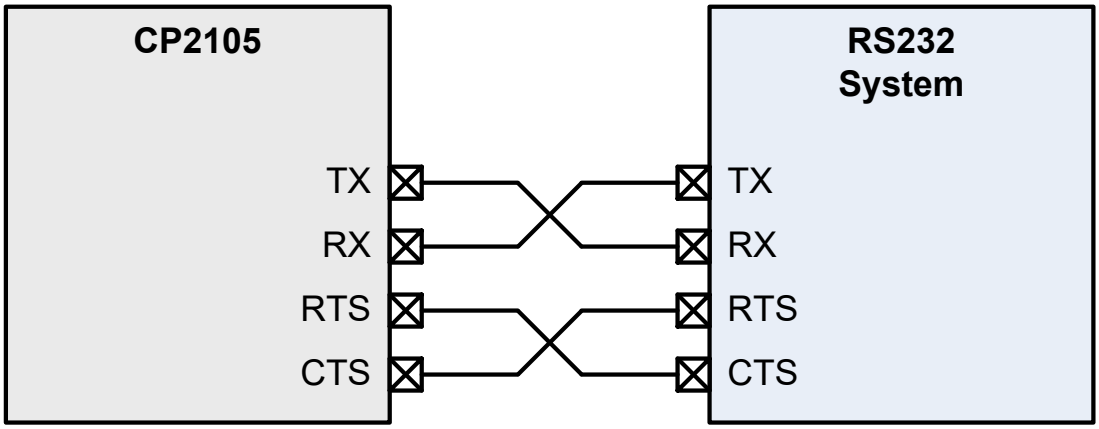


Figure 7. Hardware Flow Control Typical Connection Diagram

9. One-Time Programmable ROM

The CP2105 includes an internal one-time programmable ROM that may be used to customize the USB Vendor ID (VID), Product ID (PID), Product Description String, Power Descriptor, Device Release Number, Interface Strings, and Device Serial Number as desired for OEM applications. If the programmable ROM has not been programmed, the default configuration data shown in Table 13 and Table 14 is used.

Table 13. Default USB Configuration Data

Name	Value
Vendor ID	10C4h
Product ID	EA70h
Power Descriptor (Attributes)	80h (Bus-powered)
Power Descriptor (Max. Power)	32h (100 mA)
Release Number	0100h (Release Version 01.00)
Serial String	Unique 8 character ASCII string (16 characters maximum)
Product Description String	“CP2105 USB to UART Bridge Controller” (47 characters maximum)
ECI Interface String	“Enhanced COM Port” (32 characters maximum)
ECI Operating Mode	GPIO mode
SCI Interface String	“Standard COM Port” (32 characters maximum)
SCI Operating Mode	GPIO mode

Table 14. Default GPIO, UART, and Suspend Configuration Data

Name	Value
GPIO.0_ECI/DTR_ECI	GPIO Input
GPIO.1_ECI/DSR_ECI	GPIO Input
GPIO.0_SCI/DCD_SCI	GPIO Input
GPIO.1_SCI/DTR_SCI	GPIO Input
GPIO.2_SCI/DSR_SCI	GPIO Input
Flush_Buffers	Flush ECI and SCI TX and RX FIFO on open
$\overline{\text{SUSPEND}}$/RI_ECI	Push-pull, Active-Low
$\overline{\text{SUSPEND}}$/RI_SCI	Push-pull, Active-Low
RS-485 Level	Active-High

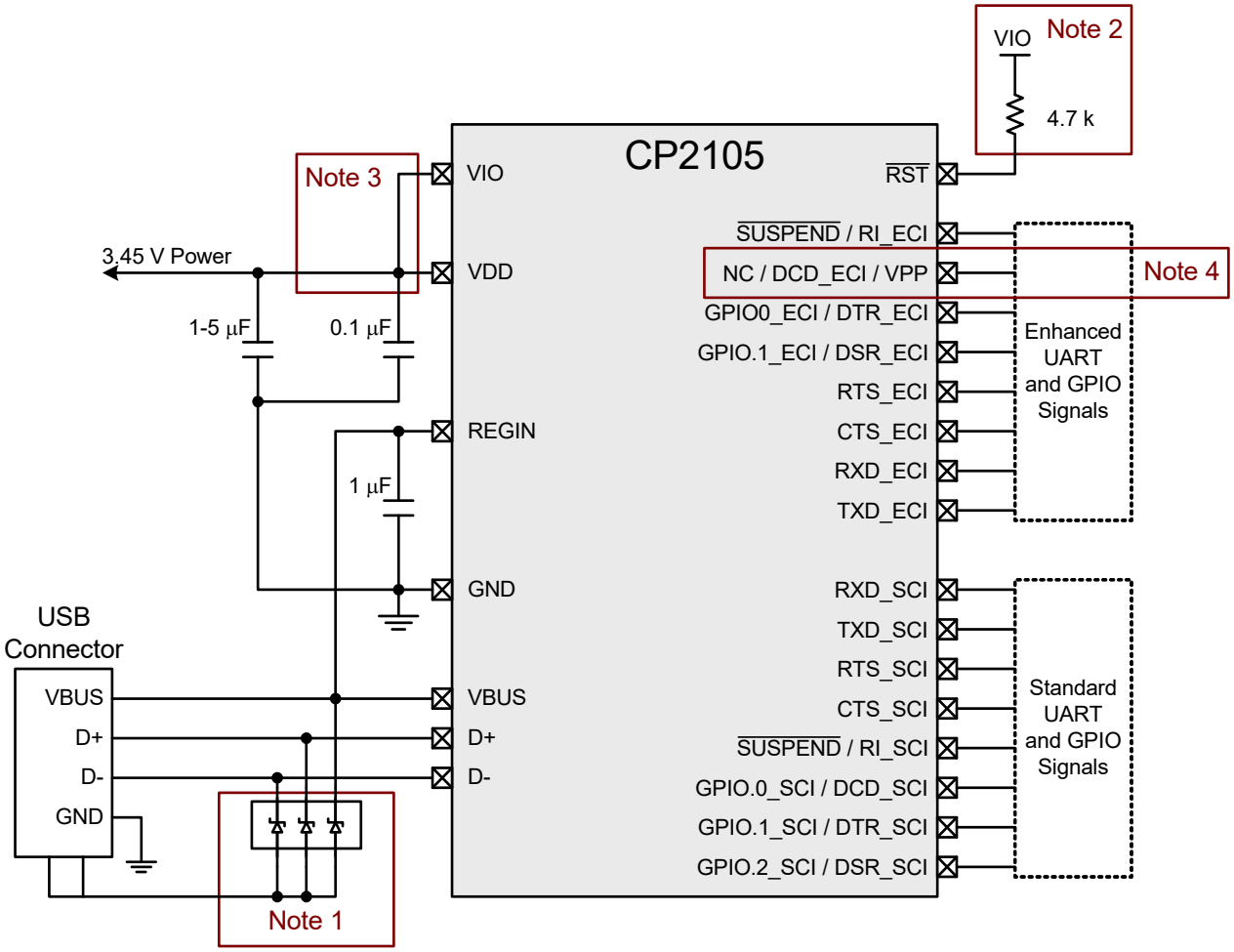
While customization of the USB configuration data is optional, customizing the VID/PID combination is strongly recommended. A unique VID/PID combination will prevent the driver from conflicting with any other USB driver from a different manufacturer’s product. A vendor ID can be obtained from www.usb.org or Silicon Labs can provide a free PID for the OEM product that can be used with the Silicon Labs VID. Device serialization is done at the factory to guarantee the ability to uniquely identify a specific device on the USB bus and other applications. This is accomplished by setting the serial number descriptor string that may be queried by the host. By default, a unique 32-bit serial number will be generated for each device at the factory. This number will be converted to an eight-character hexadecimal string. Custom serialization can also be requested.

The configuration data ROM can be programmed by Silicon Labs prior to shipment with the desired configuration information. It can also be programmed in-system over the USB interface by adding a capacitor to the PCB. If the configuration ROM is to be programmed in-system, a 4.7 µF capacitor must be added between the NC/DCD_ECI/VPP pin and ground. No other circuitry should be connected to NC/DCD_ECI/VPP during a programming operation, and V_{DD} must remain at 3.3 V or higher to successfully write to the configuration ROM.

10. Voltage Regulator

The CP2105 includes an on-chip 5 to 3.45 V voltage regulator. This allows the CP2105 to be configured as either a USB bus-powered device or a USB self-powered device. A typical connection diagram of the device in a bus-powered application using the regulator is shown in Figure 8. When enabled, the voltage regulator output appears on the V_{DD} pin and can be used to power external devices. See Table 5 for the voltage regulator electrical characteristics.

If it is desired to use the regulator to provide V_{DD} in a self-powered application, the same connections from Figure 8 can be used, but connect REGIN to an on-board 5 V supply, and disconnect it from the VBUS pin. In addition, if REGIN may be unpowered while VBUS is 5 V, a resistor divider shown in Note 5 of Figure 9 is required to meet the absolute maximum voltage on VBUS specification in Table 1.

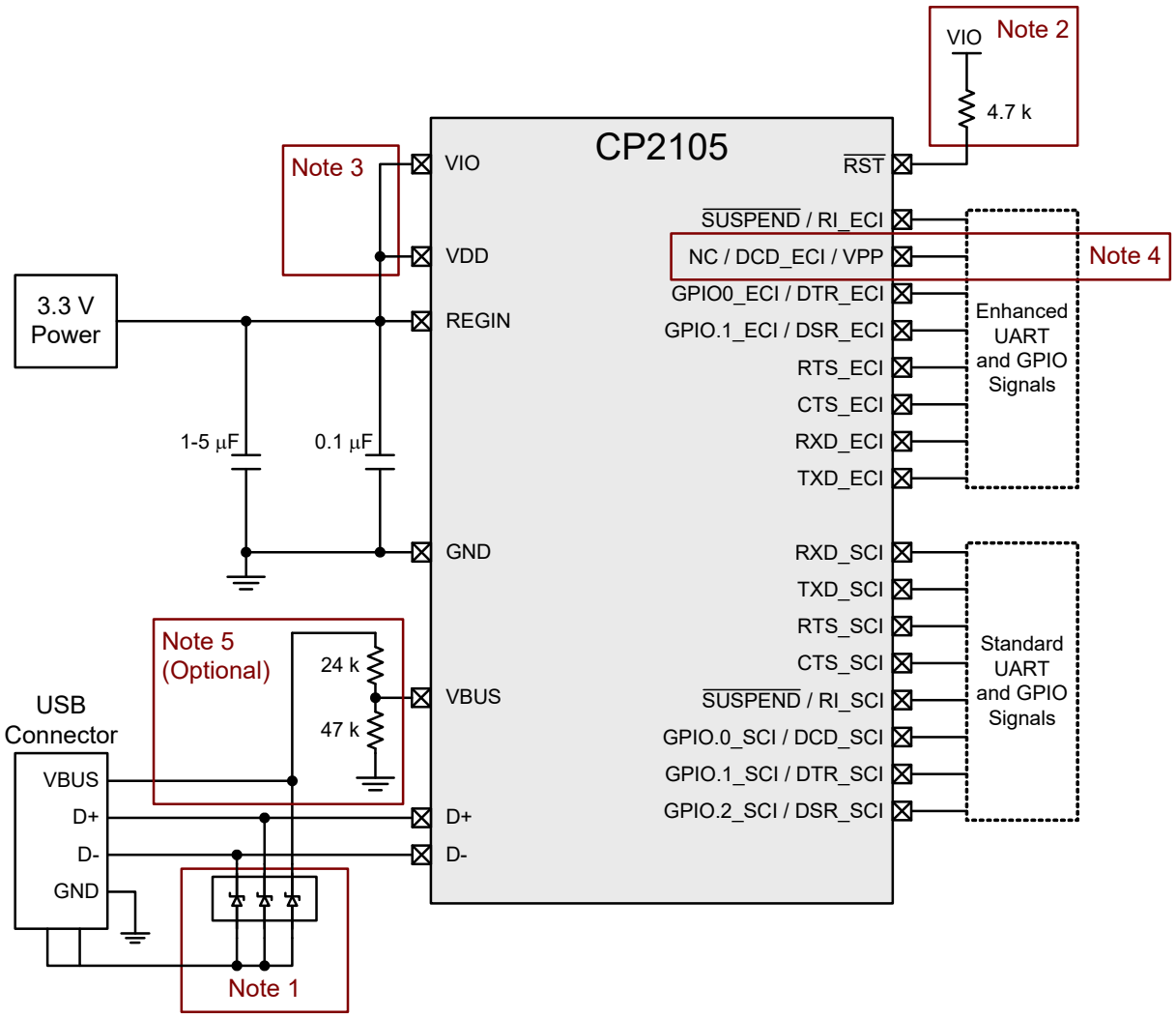


Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.
Note 2 : An external pull-up is not required, but can be added for noise immunity.
Note 3 : VIO can be connected directly to VDD or to a supply as low as 1.8 V to set the I/O interface voltage.
Note 4 : If configuration ROM is to be programmed via USB, a 4.7 µF capacitor must be added between NC / DCD_ECI / VPP and ground. During a programming operation, the pin should not be connected to other circuitry, and VDD must be at least 3.3 V.

Figure 8. Typical Bus-Powered Connection Diagram

Alternatively, if 3.0 to 3.6 V power is supplied to the V_{DD} pin, the CP2105 can function as a USB self-powered device with the voltage regulator bypassed. For this configuration, the REGIN input should be tied to V_{DD} to bypass the voltage regulator. A typical connection diagram showing the device in a self-powered application with the regulator bypassed is shown in Figure 9.

The USB max power and power attributes descriptor must match the device power usage and configuration. See application note “AN721: CP21xx Device Customization Guide” for information on how to customize USB descriptors for the CP2105.



Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.
Note 2 : An external pull-up is not required, but can be added for noise immunity.
Note 3 : VIO can be connected directly to VDD or to a supply as low as 1.8 V to set the I/O interface voltage.
Note 4 : If configuration ROM is to be programmed via USB, a 4.7 µF capacitor must be added between NC / DCD_ECI / VPP and ground. During a programming operation, the pin should not be connected to other circuitry, and VDD must be at least 3.3 V.
Note 5 : For self-powered systems where VDD and VIO may be unpowered when VBUS is connected to 5 V, a resistor divider (or functionally-equivalent circuit) on VBUS is required to meet the absolute maximum voltage on VBUS specification in the Electrical Characteristics section.

Figure 9. Typical Self-Powered Connection Diagram (Regulator Bypass)

11. CP2105 Device Drivers

There are two sets of device drivers available for CP2105 devices: the Virtual COM Port (VCP) drivers and the USBXpress Direct Access drivers. Only one set of drivers is necessary to interface with the device.

The latest drivers are available at http://www.silabs.com/products/mcu/Pages/SoftwareDownloads.aspx.

11.1. Virtual COM Port Drivers

The CP2105 Virtual COM Port (VCP) device drivers allow a CP2105-based device to appear to the PC's application software as two COM ports. Application software running on the PC accesses the CP2105-based device as it would access two standard hardware COM ports. However, actual data transfer between the PC and the CP2105 device is performed over the USB interface. Therefore, existing COM port applications may be used to transfer data via the USB to the CP2105-based device without modifying the application. See application note “AN197: Serial Communications Guide for the CP210x” for Example Code for Interfacing to a CP2105 using the Virtual COM drivers.

11.2. USBXpress Drivers

The Silicon Labs USBXpress drivers provide an alternate solution for interfacing with CP2105 devices. No serial port protocol expertise is required. Instead, a simple, high-level application program interface (API) is used to provide simpler CP210x connectivity and functionality. The USBXpress for CP210x Development Kit includes Windows device drivers, Windows device driver installer and uninstallers, and a host interface function library (host API) provided in the form of a Windows dynamic link library (DLL). The USBXpress driver set is recommended for new products that also include new PC software. The USBXpress interface is described in application note “AN169: USBXpress Programmer's Guide.”

11.3. Driver Customization

In addition to customizing the device as described in "6. Asynchronous Serial Data Bus (UART) Interfaces" on page 12, the drivers and the drivers installation package can be also be customized. See application note “AN220: USB Driver Customization” for more information on generating customized VCP and USBXpress drivers.

Important Note: The VID/PID in the drivers must match the VID/PID in the device for the drivers to load properly then the device is connected to the PC.

11.4. Driver Certification

The default drivers for the CP2105 are Microsoft Windows Hardware Quality Labs (WHQL) certified. The certification means that the drivers have been tested by Microsoft and their latest operating systems will allow the drivers to be installed without any warnings or errors.

The customized drivers that are generated using the AN220 software are not automatically certified. To become certified, they must go first through the Microsoft Driver Reseller Submission process. Contact Silicon Labs support for assistance with this process.

12. Relevant Application Notes

The following Application Notes are applicable to the CP2105. The latest versions of these application notes and their accompanying software are available at www.silabs.com/interface-appnotes.

- **AN721: CP21xx Device Customization Guide**. This application note describes how to use the AN721 software CP21xxCustomizationUtility to configure the USB parameters on the CP21xx devices.
- **AN169: USBXpress Programmer's Guide**. This application note describes the USBXpress API interface and includes example code.
- **AN197: Serial Communications Guide for the CP210x**. This application note describes how to use the standard Windows COM port function to communicate with the CP210x and includes example code.
- **AN220: USB Driver Customization.** This application note describes how to use the AN220 software to customize the VCP or USBXpress drivers with OEM information.
- **AN223: Runtime GPIO Control for CP210x.** This application note describes how to use the CP210xRuntime DLL to control the CP210x GPIO.

13. Document Change List

Revision 0.1 to Revision 0.5

- Updated ordering part number on page 1.
- Updated electrical specifications throughout Section 2.
- Added information on VPP pin in Section 3.
- Added Section 7.
- Updated Section 8.
- Updated Section 9.

Revision 0.5 to Revision 1.0

- Removed preliminary language.

Revision 1.0 to Revision 1.1

- Added a row for VBUS in Table 1, “Absolute Maximum Ratings,” on page 4.
- Added V_{DD} Ramp Time for Power On specification to Table 4, “Reset Electrical Characteristics,” on page 5.
- Added V_{PP} Voltage and Capacitor specifications to Table 2, “Global DC Electrical Characteristics,” on page 4.
- Updated AN144 references to AN721.
- Updated "10. Voltage Regulator" on page 18 to add absolute maximum voltage on VBUS requirements in self-powered systems.

Revision 1.1 to Revision 1.2

- Updated the programmable time for the line break in "6.1. ECI Baud Rate Generation" on page 13.
- Updated the information about serialization of CP210x in"9. One-Time Programmable ROM" on page 17.

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SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

www.silabs.com